Spin Valves for Reconfigurable Logic Devices

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Abstract

Spin valves are ferromagnetic nanostructures whose electrical resistance can be tuned either by an applied magnetic field, an electrical current, or in combination with an electrical current through thermal excitation. A spin valve consists of at least three layers, two ferromagnetic layers, which are separated by a non-magnetic layer. The electrical resistance of a spin valve depends on the orientation of the magnetization in both ferromagnetic layers. Two configurations are relevant for applications of spin valves in logic and memory devices, parallel and antiparallel alignment of the magnetizations relative to each other. Both correspond to two different resistances, which can represent Boolean values 0 and 1. The electrical resistance of a spin valve can be explained with the giant magnetoresistance (GMR) effect and the tunneling magnetoresistance (TMR) effect, respectively. Spin valves are promising candidates for future logic and memory devices, since they show principle assets compared to traditional technologies based on semiconductor-based field-effect transistors. The technological relevance of spin valves in memory and logic devices and in field-programmable gate arrays is investigated in this work. The acceptability of spin valves for applications is based on models that describe the electrical properties appropriately and efficiently, making spin valve available for circuit designers. Such models are referred to as a compact model. The established model for spin valves, the micromagnetic model, describes the magnetization dynamics in the ferromagnetic layers of the spin valve; it is too generic and not suited for circuit design based on spin valves. In this thesis state-of-the-art compact models for spin valves are reviewed. Following a common approach for compact models in the literature, two different electrical circuits are depicted. Both mimic the most relevant characteristic of a spin valve, the hysteresis of its electrical resistance, but at different levels of abstraction following Gajski and Kuhn's Y chart. The first circuit approximates the hysteresis of a real spin valve, but is simpler than other circuits in the literature. Two case studies indicate the flexibility of the circuit. The feasibility of logic gates based on spin valves is studied employing the circuit and picking up the case studies again. The second circuit allows for the simulation of a spin valve's hysteresis at a tunable precision. The latter circuit is an enhancement compared with recently published works in the literature on the same topic. The circuits were simulated with a free available version of SPICE, the de facto standard for circuit simulation.

Zusammenfassung

Spinventile sind ferromagnetische Nanostrukturen, deren elektrischer Widerstand mithilfe eines Magnetfeldes, eines elektrischen Stromes oder in Verbindung damit durch Aufheizen eingestellt werden kann. Ein Spinventil besteht wenigstens aus drei Schichten; dabei handelt es sich um zwei ferromagnetische Schichten, die durch eine weitere Schicht getrennt sind. Der elektrische Widerstand eines Spinventils hängt von der Ausrichtung der Magnetisierungen in den ferromagnetischen Schichten ab. Zwei Konfigurationen sind von besonderem Interesse für Anwendungen: Die parallele und antiparallele Ausrichtung der Magnetisierungen zueinander. Beide Konfigurationen führen zu unterschiedlichen Widerständen, mit denen sich die Booleschen Wahrheitswerte 0 und 1 repräsentieren lassen. Der elektrische Widerstand eines Spinventils beruht auf dem gigantischen Magnetwiderstand (GMR) beziehungsweise dem Tunnelmagnetwiderstand (TMR). Spinventile eignen sich besonders für Speicherzellen und Logikgatter, weil sie grundsätzliche Vorteile besitzen im Vergleich zu herkömmlichen Technologien, die auf Halbleiter-Feldeffektransistoren beruhen. In dieser Arbeit wird die technologische Relevanz der Spinventile für Speicherzellen, Logikgatter und Field Programmable Gate Arrays untersucht. Die Akzeptanz von Spinventilen hängt auch von der Verfügbarkeit von Modellen ab, die eine angemessene und einfache Beschreibung ihres Verhaltens erlauben. Diese Modelle erlauben den Entwurf von Schaltungen mit Spinventilen. Einfache, aber angemessene Modelle bezeichnet man als kompakte Modelle. Das gängigste Modell zur Beschreibung eines Spinventils ist das mikromagnetische Modell, das die Dynamik der Magnetisierung in den ferromagnetischen Schichten eines Spinventils beschreibt. Es eignet sich jedoch nicht, um Spinventile für den Schaltungsentwurf zu beschreiben. In dieser Arbeit wird daher der Stand der Technik der kompakten Modelle für Spinventile vorgestellt und bewertet. Einem etablierten Ansatz folgend werden zwei elektrische Ersatzschaltungen vorgestellt. Beide Schaltungen ahmen die für den Schaltungsentwurf wichtigste Eigenschaft eines Spinventils nach. Die Hysterese des Widerstandes wird mit beiden Schaltungen imitiert, allerdings auf verschiedenen Abstraktionsebenen, vergleichbar denen in Gajski und Kuhns Y-Diagramm. Durch die erste Schaltung wird die Hysterese eines Spinventils genähert durch eine rechteckförmige Hysterese. Diese Schaltung ist einfacher als die Arbeiten in der Literatur. Durch zwei Fallstudien wird die Flexibilität der Schaltung deutlich. Damit wird auch die Machbarkeit von Logikgattern untersucht. Die zweite Schaltung erlaubt es, die Hysterese bei einstellbarer Genauigkeit zu simulieren. Diese Schaltung ist eine Weiterentwicklung kürzlich veröffentlichter Arbeiten aus der Literatur. Die Schaltungen wurden mit einer frei verfügbaren Version von SPICE simuliert, dem Standardprogramm zur Schaltungssimulation.

Contents

Chapter 1

Introduction

Since the invention of the bipolar transistor in 1948, an enormous development in the fabrication of transistors led to a performance hardly anyone could imagine when microelectronics still was in its infancy. Today the semiconductor industry has become a multi-billion dollar business. According to the European Semiconductor Industry Association the worldwide sales in December 2009 for semiconductor devices were raised by 28.9% in comparison to the sales in December 2008 [1]. Innovation is required to maintain such growth rates. Scaling of devices has become an important driver in semiconductor industry. It affects all aspects of a device, like its size or the possible clock rate when switching the device. Scaling cannot be continued forever. Devices cannot get smaller and smaller forever; there are fundamental limits. And even though devices were improved up to now through scaling, some principle drawbacks remain. For example data is accessed very quickly in static random-access memory, but stored only volatile. In common nonvolatile memory technologies, like hard disks data can be accessed only very slowly or the number of write cycles is very limited (e.g. in Flash memory cells). The discovery of the giant magnetoresistance effect in the middle of the 1980's marked the dawn of *spintronics*. In contrast to conventional electronics where the charge of the electron constitutes the state variable, in spintronic devices also the spin degree of freedom is employed to represent the state variable. The technological relevance of spintronic devices is indicated for example by modern hard disks. The read head is a so-called spin valve. A spin valve is a ferromagnetic device of some nanometer in size. It consists of at least three layers, that is, two ferromagnetic layers separated by a non-magnetic layer. The relevant property of any ferromagnet is its magnetization, which can be regarded as the magnetic orientation of a tiny bar magnet. In this principle sketch the whole ferromagnetic layer corresponds to an array of these bar magnets. The magnetization in one layer is fixed, while the other magnetization can be switched with an external magnetic field or an electrical current. For the application of spin valves in electronic systems, two configurations are important: Antiparallel and parallel alignment of the magnetization in the free layer with respect to the other layer, the so-called fixed layer. Both configurations correspond to different electrical resistances. The orientation of the magnetization in both layers remains unchanged in the absence of a magnetic field or a current. The spin valve thus can directly serve as a nonvolatile memory cell. Spin valves can also be employed in logic gates and even in microwave oscillators. Hence, spin valves are

multifunctional devices. The accepted mathematical model for the description of a spin valve is the micromagnetic model. The micromagnetic model describes the magnetization dynamics of the free layer, but does not directly give information about the electrical resistance of the spin valve. For circuit design with spin valves though it is essential to have such a model. Models for the current across the non-magnetic layer have been proposed in the literature [2], but how can the behavior of a spin valve be expressed in the language of a circuit designer? In analogy to the semiconductor field-effect transistor, besides the micromagnetic model another approach for modeling a spin valve is also very popular in the literature: Mimicking the hysteresis of a spin valve with an equivalent electrical circuit. There exists a wide variety of proposals in the literature [3–5]. In this thesis two new equivalent circuits are presented, one that is much simpler than circuits from the literature. The results from simulations using this circuit are very reasonable. The second circuit is also quite simple in its assembly; it can imitate the hysteresis of a spin valve very precisely. The circuit is very flexible, as only the fitting functions and the switching points need to be changed if a different spin valve is to be mimicked. The circuit is almost insensible to loads.

This thesis is organized as follows:

In Ch. 2 an overview is given on the challenges for future devices. Problems and limits of scaling are summarized. It turns out that besides their increased performance, traditional technologies for logic and memory devices still possess principle disadvantages. Some prominent examples for alternative technologies indicate the problems of conventional technologies in the future. The technological relevance of spin valves is explained afterwards. In contrast to other technologies spin valves allow for a functional diversification. That means one device can be used for many different applications. The state of the art of memory and logic devices is recapitulated along with the physics of spin valves. Finally, the modeling of spin valves is reviewed with emphasis on compact models. It is motivated why two new approaches for a compact are still necessary.

Two different equivalent electrical circuits are described in Ch. 3. The first circuit performs a rectangular-shaped hysteresis that approximates the electrical resistance of spin valve. The dimensioning of the circuit is shown in two case studies, first for a spin valve with a small difference between parallel and antiparallel configuration and second for a spin valve with a large difference between low and high resistance. The values are guided by experimental studies of spin valves. Picking up both case studies again, the feasibility of logic gates with the equivalent circuit is evaluated.

The second equivalent circuit allows mimicking the hysteresis at a tunable accuracy. In contrast to the first circuit, this circuit models a spin valve as a device with two terminals. The feasibility of logic gates using this circuit is discussed.

The conclusion and the outlook on possible future work are presented in Ch. 4.

The netlists of the circuits related to the first equivalent circuit (with a rectangular-shaped hysteresis) and those for the second circuit (with a realistic hysteresis) can be found in the appendix.

Chapter 2

Fundamentals

In this thesis the feasibility of logic gates and memory devices based on spin valves is investigated and evaluated. The transistor was invented in order to improve the switching speed and the reliability of electronic systems. In analogy to this development, spin valves are promising candidates for future logic gates and memory devices. For the design of systems based on spin valves an application-oriented modeling approach is necessary. A compact model for spin valves that captures all relevant electrical properties at a reasonable complexity is essential for system design. After an overview of the historical developments, in this chapter the challenges for future devices are identified. A reasonable example shows a fundamental limit for the miniaturization of devices. An overview on the technological relevance of spin valves is given afterwards. Because spin valves possess some fundamental advantages over traditional technologies, the underlying physics are outlined. Finally the state of the art of compact models for spin valves is summarized and reviewed as the basis for the results in the next chapter.

2.1 Historical development

By the middle of the 1940's the main components of electronic circuits were passive devices, like resistors, inductors, and capacitors as well as active components like vacuum tubes and relays [6, 7]. A complex system at that time was the electronic controller of the B-29 aircraft which consisted of about 300 vacuum tubes. The ENIAC, one of the fastest computers back then, consisted of over $17,000$ tubes and weighted approximately $30,000$ kg [8, 9]. The first program-controlled digital computer, Konrad Zuse's Z3 from 1941 had used up to 2400 relays. On the Z3 an addition operation of two numbers takes in average 0.8 s at a clock frequency of approximately 5.3 Hz [10]. In the 1940's scientists at the Bell Laboratories in Murray Hill, New Jersey were looking for an analog of the fast, but unreliable vacuum tube and the slow electromagnetic relay. The result of their work was the invention of the bipolar transistor in 1948. In contrast, the actual analog to the vacuum tube, the field-effect transistor was proposed already in 1926, but it would not fabricated before 1952 [11–13]. Kilby and Noyce independently from each other invented the integrated circuit in 1958 based on bipolar transistors. The inventions of this era led to an enormous improvement of the reliability

and the speed of computations [6, 8]. In 1965 Gordon Moore, director of the research and development laboratories of Fairchild Semiconductor, published an article on his observation that the number of components in an integrated circuit at minimum costs roughly doubled every year [14]. By 1975 Moore, meanwhile one of the founders of Intel Corporation, himself adopted his statement to the recent developments. He now estimated that the number of transistors would double approximately every two years [15]. Eventually Moore's observation became known as "Moore's law". Up to now there has been an enormous development. Intel's 4004 microprocessor from 1971 consisted of 2,250 transistors; one of Intel's recent dual core Itanium 2 server chips has deployed 1.72 billion transistors [16].

2.2 Challenges for future devices

Moore's law is an empirical observation that allows estimating the possible increase of devices on a given area. Miniaturization is one important requirement to speed-up calculations. Without the enormous miniaturization today's mobile phones, portable computers, and supercomputers would probably not exist at this performance or look totally different. The semiconductor industry has become a multi-billion dollar business. According to a recent press release of the European Semiconductor Industry Association the worldwide sales in 2009 for semiconductor devices were US$ 226.313 billion [1]. The improvement of devices is generally referred to as scaling. Scaling of devices has become an important driver in semiconductor sales. Innovation is required to maintain the growth in this area. Basically, there are two ways of achieving innovation in the field of semiconductor-based computers (1) with improvements of the architecture and (2) with improvements of the fabrication technology and consequently the scaling of devices.

Some of the most important drawbacks of the classical von-Neumann computer architecture are:

- The sequential execution of instructions in spite of pipelining.
- The fetch phase in each execution of an instruction, even if the same instruction is executed many time in a row.
- The separation of the processor from the main memory. If the throughput of data between memory and processor is smaller than the rate at which data is processed, the processor has got to wait until data is available again. This problem is known as von-Neumann bottleneck. The problem gets worse with the ever increasing clock rates of modern processors.

There exists a wide variety of alternatives to the classical von-Neumann architecture. All aim at a higher performance by overcoming or weakening the principle drawbacks of the von-Neumann architecture. Some examples indicate this:

- Intel and other manufacturers have come up with multi-core processors. Instead of a single processing unit, two, four, eight or even more of them are available for parallel

execution. In the long run this strategy could be extended. Within its "Tera-scale Computing Program", Intel recently came up with an eighty-core processor. This processor could achieve 1.81 Tera-flops at a clock rate of 5.7 GHz [17].

- Scientists from the University of Texas at Austin, USA have proposed the TRIPS architecture[1] [18]. The authors have identified requirements for future computer architectures, such as power-efficient performance. A main characteristic of the TRIPS architecture is the direct instruction communication, where the hardware implements producer instructions whose output is directly available to consumer instructions, rather than writing the output to a register. A TRIPS machine offers an array of concurrently executing arithmetic logic units. By now, a TRIPS processor has been fabricated where a chip contains 170 million transistors spread over two processors [19].

- The Cell Broadband Engine is an architecture developed at IBM's research laboratories [20]. Instead of duplicating the same core on a chip, the Cell processor is a heterogeneous architecture. There is a mix of execution elements optimized for a range of applications. Applications are partitioned into components. Each component is executed on the most appropriate execution element. The Cell Broadband Engine consists of a 64 Bit processor and eight so-called synergistic processor elements, each with a local memory. Each processing unit is connected with a high performance bus.

- If the computer is designed for a single application only, its hardware can be optimized for this purpose. However, once the circuit is fabricated on a chip, it can no longer be modified. This type of computer is called an application-specific integrated circuit. It leads to a much better performance than a general-purpose processor or a domain-specific processor. From this point of view there arises a conflict between the flexibility of a general-purpose processor and the performance of an application-specific integrated circuit. Scientists like Hartenstein have proposed the approach of a reconfigurable computer that offers both, more performance than a general-purpose processor and more flexibility than an application-specific integrated circuit [21]. In a reconfigurable computer the hardware is configured for every task. The device structure will be reconfigured completely or in part depending on the succeeding task. Some years ago Hartenstein gave an overview on reconfigurable architectures in an influential paper [21]. An important requisite for a reconfigurable computer architecture is reconfigurable hardware, in particular field-programmable gate arrays. Spin valves overcome the drawbacks of conventional technologies like SRAM or Flash memory and are hence excellent candidates for field-programmable gate arrays.

The focus of this thesis lies in the evaluation of alternative technologies for logic gates and memory cells rather than in a profound review of the state-of-the-art of computer architecture. Besides improvements of the architectures of technical systems, improvements of the fabrication technology and consequently scaling of devices have led to an increase of their performance. Widely used technologies to implement memory cells are static random-access

[1] TRIPS stands for "Tera-op[erations], Reliable, Intelligently adaptive Processing System"

memory (SRAM), dynamic random-access memory (DRAM), Flash memory, and magnetic hard-disks. An SRAM cell consists of two coupled inverters [22, 23]. Usually, an SRAM cell consists of six transistors, leading to a comparatively large cell area [24]. In a DRAM cell, the stored information is represented through the charge of a capacitor [25, 26]. The leakage current of the capacitor leads to a small retention time [24]. Flash memory is based on the so-called floating-gate transistor [27–29]. To alter the stored bit in a Flash cell, the electric charge within the floating gate has got to be changed by either injecting electrons into the floating gate or by removing electrons, respectively. These mechanisms limit the lifetime of the Flash cell. Main drawbacks of Flash memory are thus the long write/erase time and the small number of write cycles before the device will not work reliable anymore. The durability of a stored bit in a Flash cell is approximately 10^9 times worse than in an SRAM cell. The main drawback of hard-disks is their access time. These currently lie in the order of ms [30].

Scaling affects all aspects of a device, like the size, power consumption or clock frequency. The scaling of field-effect transistors (MOSFETs) led to a considerable increase of their switching speed [31]. An overview of the current state of the art in device scaling is given by the International Technology Roadmap for Semiconductors (ITRS) [32]. The Roadmap is sponsored by industry associations, like the Semiconductor Industry Association or the Japan Electronics and Information Technology Industries Association. Groups of experts work on different topics related with the semiconductor industry in order to collect recent characteristics of semiconductor devices. The ITRS aims at enabling technology assessment and is a reliable source of data. The recent edition of ITRS is that of 2009 [32]. The ITRS also gives an estimate on the scalability of devices, like a DRAM or a Flash memory cell. For DRAM cells the scaling is expressed for example through the half pitch which is half of the distance between two neighboring cells. It is projected that by 2024 the half pitch for DRAM will be at 8.9 nm [33]. Furthermore the ITRS names requirements that future devices should match. The drawbacks of the aforementioned technologies can be weakened through scaling. The area required for an SRAM cell would shrink for example if the size of the transistors would could be reduced. With miniaturization however manufacturers have to face problems in the following areas:

- leakage currents [34–40]
- thermal dissipation [35, 36, 40–42]
- power efficiency [36, 37, 43–45]
- reliability / statistical variability [9, 34–36, 39, 42, 45, 46]
- energy per bit [47]
- cost [40]
- lithography [9, 35, 40]
- delays on interconnections [48, 49]

With the miniaturization the quantum nature of the electrons becomes more and more dominant within the semiconductor transistors. Powell argues that Heisenberg's uncertainty relation defines the limit to miniaturization [35]. A more reasonable minimum scale of length in a solid is defined by the *Fermi wavelength* λ_F. The highest energy level for free electrons in a solid in the ground state is the Fermi energy. It is the energy on the surface of a sphere with radius k_F. The Fermi wavelength can be calculated from $k_F = 2\pi/\lambda_F$; for copper $\lambda_F = 4.6199 \cdot 10^{-10}$ m [50]. Powell's formulation of Moore's law yields that miniaturization converges to the Fermi wavelength for copper by 2021. For the calculation the 45 nm-technology node of 2008 was assumed. The lattice constant for silicon could be considered as another comprehensible estimate for the limits of miniaturization. The lattice constant of silicon is 5.43 nm [50].

The transistor was invented in order to improve the reliability and switching speed in electronic circuits. It allowed furthermore increasing the number of components in a circuit, that is, the complexity of the circuit. Along with the miniaturization of transistors came an increase of their performance. It seems likely that the enormous growth rates of the semiconductor industry could be maintained if further miniaturization would be possible. Miniaturization though becomes more and more complicated and researchers have identified fundamental limits as shown above. In spite of the improvements due to miniaturization, today's dominating technologies for memory devices show fundamental drawbacks. From a principle point of view, an ideal memory cell would be simple in its assembly, as it would consist of one device only. The data would be stored nonvolatile with a high data retention time and a small access time. The cell would show almost no material fatigue and would work with a low operating voltage. If it is possible to build up logic gates with the same device that is used for memory cells, this opens up new possibilities for reconfigurable computing devices. The number of gates or the size of a memory block could be freely allocable within the total number of devices. Functional diversification is identified to be one important challenge for future devices in the ITRS ("Moore's Law and More") [33]. It means that one device can perform different functionalities. There exists a wide variety of alternative technologies to implement memory cells. In the chapter on emerging research devices of the ITRS [51] several emerging memory technologies are named with demonstrated and projected parameters. Among these memory technologies are current-driven spin valves. Other promising technologies for example are:

- *Ferroelectric random-access memory cells (FeRAM).* The FeRAM cell consists of a capacitor with a ferroelectric layer as the dielectric and a pass transistor; thus the structure is similar to a DRAM cell. A voltage pulse is applied to set the electric polarization of the ferroelectric layer. Binary states can be distinguished through the charge of the ferroelectric capacitor [52]. Data is readout by applying a voltage pulse, which subsequently requires reprogramming. Recently a 128 Mb FeRAM device was presented [53]. A read/write voltage of 220 mV was achieved at a cell size of 0.252 µm^2. The clock frequency was 400 MHz. *Ferroelectric field-effect transistors* on the other hand have a gate dielectric made of a ferroelectric material. FeFETs allow for a non-destructive read-out in contrast to ferroelectric capacitors, and show a better scalability due to their sim-

pler structure [54]. Takahashi *et al.* demonstrated a ferroelectric CMOS inverter [55]. FeRAM is a nonvolatile memory technology, because the ferroelectric polarization is conserved after programming.

- *Carbon nanotubes.* Carbon nanotubes (CNT) have gained attention because of their splendid electrical properties, such as a high carrier mobility [56]. A prominent example for a nanomechanical memory device is described by Rueckes *et al.* [57]. Here carbon nanotubes are used for both, the memory cells and the connections between them. A memory cell is based on a suspended matrix of nanotubes. Logic gates based on field-effect transistors with carbon nanotubes were fabricated by Bachtold *et al.* [58]. A field-effect transistor that employs a graphene quantum dot of 10 nm in width was recently demonstrated [59].

- *Phase-change memory.* The amorphous and crystalline state of a bulk material differ from each other. The optical contrast between both states is exploited in re-writable CDs and DVDs [60]. The phase change is induced by Joule heating in the device. The two different phases correspond to two different electrical resistances. The phase-change device is fabricated for example with a chalcogenide (e.g. sulfur, selenium, and tellurium) [61]. The crystalline phase has a low resistance (in the range of some kΩ), whereas the amorphous phase has a high resistance (in order of some MΩ). Phase-change memory is nonvolatile, shows a good scalability and performance and can be fabricated in a low-cost CMOS process [61].

- *Molecular memories.* Single molecules can be used as electronic switches and storage elements. The molecules can be tailored by chemical synthesis. Self-organizing molecules promise a high storage density [62]. Self-organizing devices could be used to cheaply achieve a high degree of parallelism for computations. Green *et al.* describe a 160 kbit molecular electronic memory circuit [63]. They could achieve 10^{11} devices per cm^2. According to Green *et al.* this is roughly the same density of devices projected for DRAM in 2020.

Besides these examples magnetic nanostructures also have gained attention, because they fulfill the requirements for ideal cells for memory and logic. In magnetic devices not only the charge of an electron is used to represent the state variable, but also the spin of the electron. This field of research is known as magnetoelectronics or more recently *spintronics* [64–66]; an early proposal on how the spin degree of freedom could be utilized in a device is the spin transistor by Datta and Das [67]. Ferromagnetic nanostructures also encounter challenges and limits. Problems are due to quantum and temperature fluctuations [68]. The most prominent example is the *superparamagnetic effect*, which limits for example the size of magnetic grains in hard disks. There exists a critical size for the grains, which depends on the uniaxial anisotropy and the volume of the particle [69, 70]. Below the critical size, the magnetization of a particle is not stable and is switched randomly due to thermal excitation. Common strategies to shift the superparamagnetic limit include materials with higher anisotropy or the usage of single domain patterns [71].

There is a variety of novel concepts for magnetic storage devices. Magnetic vortices and antivortices could be employed to constitute a memory cell [72, 73] or logic gates [74]. Much attention is devoted to memory cells and logic gates based on magnetic domain walls [75, 76]. S-shaped structures were lately proposed for logic gates [77]. Magnetic nanodots are also frequently proposed for logic devices [78, 79]. Promising candidates for memory and logic devices are spin valves [80]. These are ferromagnetic devices in the nanometer scale whose electrical resistance can be changed either due to an applied magnetic field or an electrical current. Of particular interest for circuit design are the electrical properties of spin valves. Their behavior may be extracted from experimental data.

In this thesis models for the description of a spin valve's behavior are evaluated and two equivalent circuits are proposed. The circuits mimic its most important property, the electrical resistance. The resistance shows a hysteresis-like behavior; that means the electrical resistance does not depend on the input signal alone, but also on the previous configuration of the spin valve.

The key property of any ferromagnetic sample is its magnetization. The magnetization at each position in the sample can be regarded as a magnetic orientation just like in an array of tiny bar magnets. The orientation of the magnetization in one layer of the spin valve is fixed while the orientation of the magnetization in the other layer can be switched. The latter layer is called the free layer. With a spin valve binary symbols can be represented through the orientation of the magnetizations in the two ferromagnetic layers relative to each other, since both correspond to two different resistances. With the discovery of the giant magnetoresistance (GMR) effect, spin valves came into the focus of many scientists [66, 81, 82]. In 2007 Peter Grünberg and Albert Fert were awarded the Nobel Prize in Physics for this discovery [83]. Today's read heads in hard-disks are mostly GMR heads.

The decision whether spin valves are suited for computing devices depends on whether they achieve the features of today's semiconductor devices. Their ability of performing logical and storage operations is also important. The ITRS lists projected and demonstrated parameters of spin valves. They indicate the potential of spin valves in memory and logic devices. The most likely scenario is a combination of spin valves and MOSFET-based technologies, bringing together the assets of both worlds[2]. As mentioned above ("Moore's Law and More"), functional diversification is believed to be an important issue for future technologies for memory and logic devices. Spin valves allow for a diversification. It has been demonstrated that spin valves can be used for

- RF oscillators [84–86]
- biochips [87, 88]
- logic devices in space applications (due to their radiation hardness) [89, 90]

[2]MOSFET stands for metal-oxide-semiconductor field-effect transistor.

- sensors (e.g. read-head in hard-disks)

besides their use in logic and memory devices (cf. Sec. 2.3). Spin valves may overcome the memory hierarchy in computers [91]. The memory hierarchy describes the dichotomy between the cost and the performance of today's memory technologies. Hard-disks allow for a low cost storage, but show a large access time (see above). Technologies like SRAM have a small access time, but are too expensive for mass storage systems. The acceptability of spin valves also relies on the availability of models that allow simulations of large scale circuits, as a realistic and practical approach. In Sec. 2.5 the state of the art in modeling and simulation is described. In Ch. 3 two models of the spin valve's hysteresis are presented that allow for the simulation of complex systems based on spin valves.

2.3 Field-programmable gate arrays based on spin valves

Spin valves can be used in combination with technologies based on the field-effect transistor to improve the features of a logic gate or a memory cell. For example, a field-effect transistor serves as a current source for the spin valve. According to the data from the ITRS spin valves already have comparable features with respect to SRAM, DRAM, and Flash memory or are expected to have [92]. Using spin-polarized currents helps reducing the current to write data [93]. A switching time of 100 ps was demonstrated with a current-driven MRAM cell [94], which is in the same order as the switching time for SRAM. Xu *et al.* depict a 256 Mb MRAM chip in 45 nm-process technology [95]. Another chip with current-driven MRAM exhibits a write time of 100 ns and a read time of 40 ns [96]. One proposal shows that the time to write a bit can be reduced to 2 ns [97]. In 2007 an MRAM chip was fabricated in a 28 nm-process resulting in a feature size of only 6 F^2 (compared to 45 F^2 for MRAM in the current ITRS) and a sensing current of approximately 10 µA [98]. A clock frequency up to 500 MHz was demonstrated by Sakimura *et al.* [99]. There exists a number of works on memory modules based on field-driven spin valves [100–103].

At the 1960 International Solid-State Circuits Conference Proebster and Oguey proposed to use the magnetization in a Permalloy film as a memory cell and a logic gate [104]. The idea of implementing a logic gate with spin valves is propagated by several publications [64, 105, 106]. Today two different approaches are dominant. The first approach is to use a single spin valve. A Boolean input is represented through the direction (+ or −) of an electric current. For each input there is a separate wire connected to the spin valve. The currents on each line are summed up and the resulting Oersted field or spin-transfer torque switches the magnetization in the free layer (cf. Sec. 2.4). In between two sensing terminals the resistance of the spin valve is measured. The logical value 1 is represented through high resistance, that is, the antiparallel alignment of the magnetizations of both layers, and the logical 0 through low resistance which corresponds to a parallel alignment of the magnetizations of the layers. Similar to a memory cell, the input wires of the logic gate serve as the "bit-line"; the voltage between the sensing terminals is a selection signal like the one on a "word-line". Several works on logic gates based on spin valves follow this approach [107–111]. All relevant Boolean functions,

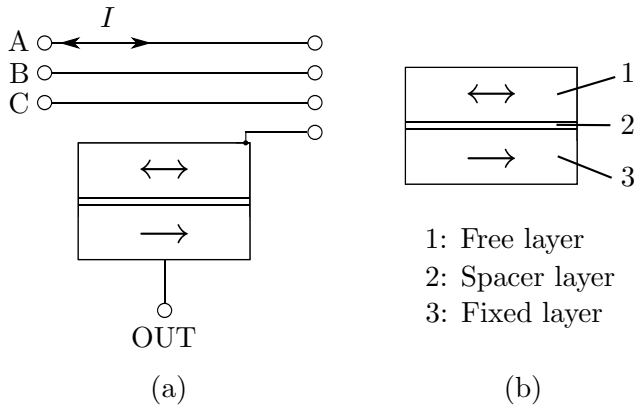


Figure 2.1: (a): Scheme of the logic gate based on a spin valve as introduced by Ney *et al.* [107]. On each of the input lines A and B a current can flow, each of equal magnitude. The direction of the current determines the orientation of the magnetization in the spin valve. Each of these currents, I_A and I_B, alone is not able to switch the magnetization in the free layer, only I_A+I_B. Together with I_A and I_B, a current I_C on the third input line C can switch the orientation of the magnetization in the fixed layer. This corresponds to programming the logic function of the gate. The output can be measured between an electrode attached to the top of the spin valve and the output terminal OUT. Originally Ney *et al.* assumed that the magnetizations are switched through Oersted fields which are generated through the currents on the input lines. (b): Layers of a spin valve.

like AND, OR, NAND, and NOR can be implemented. The concept is schematically shown in Fig. 2.1. Complex logic devices have been demonstrated following this concept [112, 113].

The second approach to implement logic gates was proposed by Richter *et al.* and uses four spin valves to implement a logic gate, forming an input and a reference branch [114–116]. Such a logic gate is shown in Fig. 2.2. The input branch is a series of two spin valves, whose resistance is determined or programmed by the two inputs. The reference branch also consists of two spin valves in series. Their resistance is determined before the gate can be used and remains unchanged during operation. In an experiment the difference between both states is measured to be of the order of 2 kΩ [114]. A similar approach comparing the resistance of two branches was published by Hassoun *et al.* in 1997 [117]. Once the resistances of the spin valves are programmed, a sensing current is applied to both, the reference and the input branch. The resulting voltage drop between the input and the reference branch is the representation of the Boolean output of the gate. Similar to the first approach, a logical 1 is represented through high resistance which corresponds to an antiparallel alignment of the magnetizations relative to each other. A logical 0 is represented through low resistance. Proper operation of logic gates (NAND and NOR) has been demonstrated in experiments; special attention is given to the impact on the statistical variation of the magnetoresistance due to statistical variation during the fabrication and to the scalability of the devices [118–120]. In general the logic gates based on spin valves need additional amplification. The output voltage can

be in the range of mV only [114]. The output voltage of a logic gate however should be able to drive another gate. A simple solution is to use a comparator circuit: If the gate's output voltage is below an a priori chosen threshold, the output is converted to a convenient voltage to represent logical 0. Similarly the output of the gate is converted in order to comply with a desired voltage level for logical 1.

Richter *et al.* employ four spin valves for a single logic gate, whereas the logic gate of Ney *et al.* is constituted by a single spin valve only. The asset of Richter's gate however is that the authors experimentally prove proper operation of their logic gates taking into account also the influence of statistical variations of the fabrication. The problem of driving a number of other spin valves with the output signal of a spin valve is common to both concepts and needs to be solved.

The significance of spin valves as reconfigurable logic devices led to a multitude of publications on spin valves in field-programmable gate arrays (FPGA). An FPGA basically consists of an array of logic gates, programmable interconnections, input/output devices, and memory cells [121]. The logic gates are often implemented through memory cells as well as the interconnections [122]. With a number of inputs any combinational Boolean function can be mimicked with a memory cell. Such an addressable memory cell is often called a *look-up table*. They allow more flexibility than a rigid number of NAND and NOR gates. The idea of an FPGA is to directly configure the hardware depending on the specific application. A conventional FPGA is usually built with SRAM cells [122]. Computing with FPGAs combines the flexibility of a software-programmed computer and the performance of an application-specific integrated circuit [21, 123]. The term of a field-programmable logic gate in connection with spin valves can be traced back to 1997 [117]. This concept has been verified experimentally [124]. An influential work was published by Black *et al.* [106]. The authors performed simulations in SPICE of a flip-flop and could verify their design with an experimental study [125]. In the simulation the behavior of a spin valve was expressed in terms of an equivalent circuit that mimics measured characteristics like the hysteresis. Here an SRAM cell is coupled with several spin valves. Recent works show studies on look-up tables, either by experiment or simulation [126–128]. In some articles the design of a look-up table is discussed employing a so-called *magnetic tunnel junction* (MTJ). This is a spin valve where the spacer layer in between the ferromagnetic layers is an insulator [129–132]. Another approach is to express the resistance of the spin valve with two Ohmic resistors [89, 90, 133]. Look-up tables with magnetic tunnel junctions that utilize thermally assisted switching are also considered in the literature [134, 135].

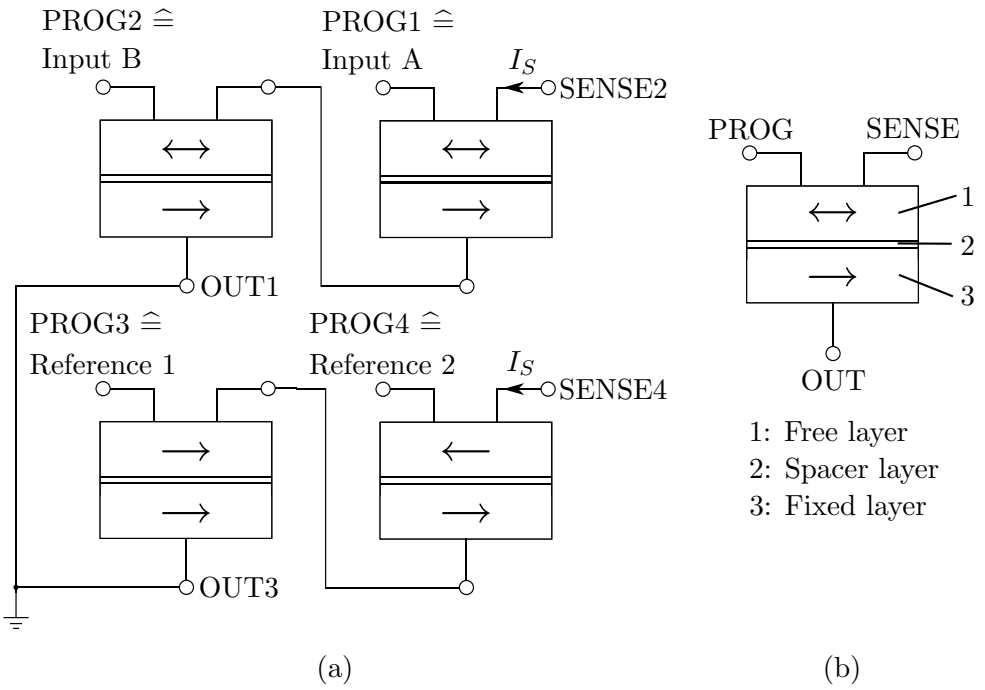


Figure 2.2: (a): Scheme of the logic gate based on spin valves as introduced by Richter *et al.* [114]. The *input branch* is the series of the two upper spin valves. Their resistance is determined, that is, programmed by the two inputs, A and B. The lower spin valves form the so-called *reference branch*. Their resistance is determined before the gate can be used and remains unchanged during operation. In the current configuration the gate is programmed as a NAND gate. If both reference cells are programmed to the antiparallel state, the gate performs the logical NOR function. A sensing current I_S is applied at the terminals SENSE2 and SENSE4. The current causes a voltage drop over the upper and lower branch. The current must be chosen such, that it does not alter the magnetization in the spin valve. The difference between the voltage drops in both branches is the output voltage of the gate. Attention must be paid to the situation where upper and lower branch have the same resistance. If deviations of the resistances due to the fabrication of the spin valves are neglected, the corresponding output voltage is 0 V. In this case the gate is not be able to drive other gates. (b): The circuit symbol of the spin valve. The resistance of the spin valves can be measured when they form a voltage divider with an extra resistor, that is connected to the spin valve via the SENSE terminal. The output voltage that corresponds to the spin valve's resistance drops between the terminals SENSE and OUT. The terminal PROG indicates the input of the spin valve; a current is applied to switch the magnetization.

2.4 Physics of spin valves

The ancient Greeks discovered that lodestone (magnetite) attracts iron. In those days lodestone was mined in the province of Magnesia. The physical phenomenon that causes the attraction of iron and lodestone is nowadays called *magnetism* [136]. Mattis explains that the term magnetism may also have originated from a shepherd called Magnes. The use of ferromagnetic material can be traced back to the forth millennium BC. Small tubular beads made of iron were found in Sumerian and Egyptian tombs; Chinese writings from this period also mention magnetite [137].

From hard disks it is well known that data is stored nonvolatile. A bit is stored within a small-sized region on a disk that is covered with a ferromagnetic film [138]. The orientation of such a region can be changed with a coil that is positioned above the region. A current through the coil generates a magnetic field which then determines the orientation of the region on the disk. In the absence of a magnetic field the orientation of the region is conserved. Similarly the electrical resistance of a spin valve remains unchanged until it is reprogrammed.

In the following the most important concepts related to the physics of spin valves are briefly described. Where necessary, further reading is suggested to the reader.

It is the ferromagnetic materials that are used in hard disks and magnetic nonvolatile memory cells. Ferromagnetism in a solid arises because of a spontaneous magnetic moment in the material that exists even when no external magnetic field is present. The magnetic moment is caused by the spin and the orbital angular momentum of the electrons in the solid. The *magnetization* is a vector that is defined as the magnetic moment per unit volume [50]. It is the most important quantity in the context of spintronic devices. The absolute value of the magnetization in a ferromagnet is sketched in Fig. 2.3; the hysteresis is an ambiguous function of the applied field. Well distinguishable states M_R and $-M_R$ may represent logical values 0 and 1 in magnetic memory and logic devices. The total magnetic field in a ferromagnet does not only depend on an external magnetic field. The so-called *effective field* also has contributions from within the ferromagnet itself. The anisotropy field depends on the direction of the magnetization relative to the structural axis of the material. The exchange field is caused by the preference of a ferromagnet to have its magnetization aligned parallel. Ferromagnets have a stray field which also contributes to the effective field. The stray field can be made visible outside the ferromagnet for example by sprinkling iron filings around the ferromagnet. Eventually magneto-elastic interactions and magnetostriction have an influence on the effective field [139, 140]. An established model to describe the dynamics of the magnetization is the so-called *Landau-Lifshitz-Gilbert equation* [140–145]. In the micromagnetic model magneto-elastic interactions and magnetostriction are not included explicitly. The micromagnetic model allows to spatially resolve the magnetization dynamics of a spin valve. However, it is too generic from the application point of view. The simulation of a large array of spin valves using the micromagnetic model would be not manageable in a reasonable computation time. An intuitive approach to reduce the complexity of the micromagnetic model

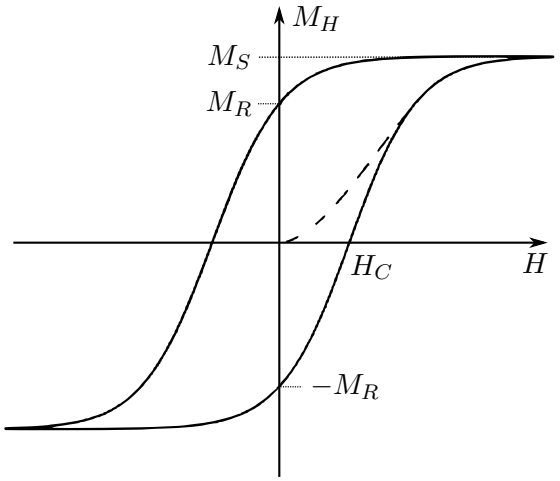


Figure 2.3: Schematic representation of the magnetization in a ferromagnet depending on the applied magnetic field. The magnetization shows a hysteresis. H is the strength of the magnetic field, M_H is the magnetization in the direction of the applied magnetic field. H_C is the *coercive field strength*; this is the field strength, where $M_H = 0$. The *remanence* is defined as the magnetization at zero field. If the applied field is swept in positive direction, the remanence is M_R; if the applied field is swept in the negative direction, the remanence is $-M_R$. M_S is the saturation magnetization, where apart from thermal excitation the magnetization is completely aligned in the direction of the applied field. If the sample is initially unmagnetized, the dashed curve is obtained during the sweep of the applied magnetic field; this curve is called initial magnetization curve. Sketch modified from reference [139].

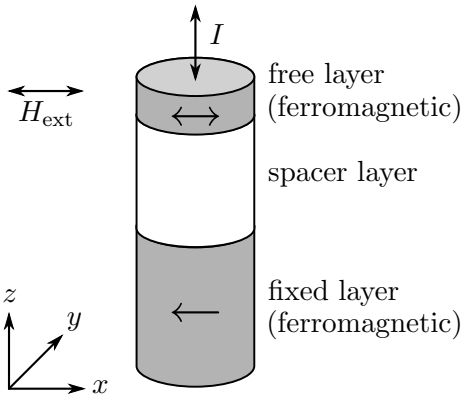


Figure 2.4: Sketch of a spin valve. The free and fixed layer are made of a ferromagnet. The spacer layer is either made of a non-magnetic metal or an oxide. The current I indicates current-induced switching. If it flows through the fixed layer first, this leads to a parallel orientation of the magnetization in the free layer with respect to the magnetization of the fixed layer; if the current flows through the free layer first an antiparallel orientation of the free layer is obtained. H_{ext} indicates field-induced switching of the magnetization in the free layer. A parallel orientation of the magnetizations corresponds to a low resistance, whereas an antiparallel orientation corresponds to a high resistance. Both configurations can be used to represent logical values 0 and 1.

is to reduce the spatial and temporal resolution of the magnetization. The resulting model is called the *macrospin model*. Such a coarsening is crucial since it reduces the accuracy of the model with respect to the magnetization dynamics in spin valves [146]. The idea that a spin valve possesses only two configurations of the magnetization of the free layer (parallel or antiparallel to the magnetization of the fixed layer) is a reduced macrospin model. However, the micromagnetic model is not a compact model in terms of Verret's quality criteria for compact models.

Spin valves are devices in the range of some nanometers in size. They consist of at least two magnetic layers with a non-magnetic conducting or insulating layer, the spacer layer, in between. The thicknesses of the layers depend on the actual assembly of the spin valve. The thicknesses lie in the order of some nm [147]. The alignment of the magnetization in one layer is fixed due to a higher coercivity. The alignment of the magnetization in the other layer can be switched; in turn this layer is called the free layer. Figure 2.4 shows the sketch of a spin valve.

Magnetoresistance effects for spin valves

For circuit design two configurations of the orientation of the magnetizations with respect to each other are assumed, parallel and antiparallel. Both can be used to represent Boolean values. The state of the magnetization in the free layer can be detected with the help of the

giant magnetoresistance effect (GMR) or the tunneling magnetoresistance effect (TMR). In the former case the spacer layer is made of a non-magnetic conducting material like copper. In the latter case the spacer layer is made of an insulator like magnesium oxide. The electrical resistance of a spin valve depends on the alignment of the magnetization in the free layer with regard to that of the fixed layer [148]. The resistance of a spin valve can be determined for instance by measuring the voltage drop due to a sensing current.

The GMR-effect was discovered by Grünberg and Fert [81, 82]. The origin of the resistance is spin-dependent scattering within a ferromagnetic layer [148, 149]: In Mott's two-channel model there exist two separate current channels for spin up and spin down electrons[3]. In a spin-polarized current the spin of a majority of electrons possesses one and the same orientation (e.g. spin up), whereas the spin of a minority of electrons possesses a different orientation. In one of the ferromagnetic layers of a spin valve majority electrons (with a spin parallel to magnetization in the layer) are almost not scattered, while minority electrons have a higher probability of being scattered.

An established model for the tunneling current through the spacer layer was proposed by Jullière who also performed experiments. A review on experiments and theory of tunneling magnetoresistance is given by Moodera and Mathon [2]. The spin of an electron is conserved during the tunneling. If the ferromagnetic layers are aligned in parallel, the tunneling probability is at highest and thus the tunneling current is at a maximum. This yields a low resistance. For the antiparallel orientation of the magnetizations in both layers, the tunneling probability and in turn the tunneling current is small. The antiparallel orientation corresponds to a high resistance.

The strength of the tunneling magnetoresistance and the giant magnetoresistance for a spin valve is usually expressed through

$$\frac{\Delta R}{R_P} = \frac{R_{AP} - R_P}{R_P}, \tag{2.1}$$

where R_P is the (lower) electrical resistance for the parallel orientation of the magnetizations of the spin valve, R_{AP} is the (higher) electrical resistance of the spin valve for the antiparallel orientation of the magnetizations in free and fixed layer.

Mechanisms for switching the free layer

The most important mechanisms for switching the magnetization in the free layer are the field-induced, current-induced, and thermally assisted switching.

[3]The splitting of electrons into spin up and spin down electrons was first discovered by Gerlach and Stern [150]. The electron configuration for silver is $4d^{10}5s$ [50].

Field-driven switching

Field-driven switching denotes the switching of the magnetization in the free layer by an applied magnetic field. It can be understood by looking at the relation between the magnetic flux density (also magnetic induction) $\boldsymbol{B}$ (in $\frac{\mathrm{kg}}{\mathrm{s}\cdot\mathrm{A}}$), the magnetization $\boldsymbol{M}$ and the magnetic field strength $\boldsymbol{H}$ (both in A/m) [140]

$$\boldsymbol{B} = \mu_0\big(\boldsymbol{H} + \boldsymbol{M}\big), \tag{2.2}$$

where $\mu_0 = 4\pi \cdot 10^{-7}\ \frac{\mathrm{kg}\cdot\mathrm{m}}{\mathrm{s}^2\cdot\mathrm{A}^2}$ is the magnetic permeability of free space [50]. By applying a magnetic field to a ferromagnet, the magnetization $\boldsymbol{M}$ is aligned in the direction $\boldsymbol{H}$, like a compass is aligned in the direction of the earth's magnetic field. A steady current through a wire generates a magnetic field. A memory cell with a field-driven spin valve is normally assembled as shown in Fig. 2.5 [100, 151]. The word line is situated on top of the spin valve,

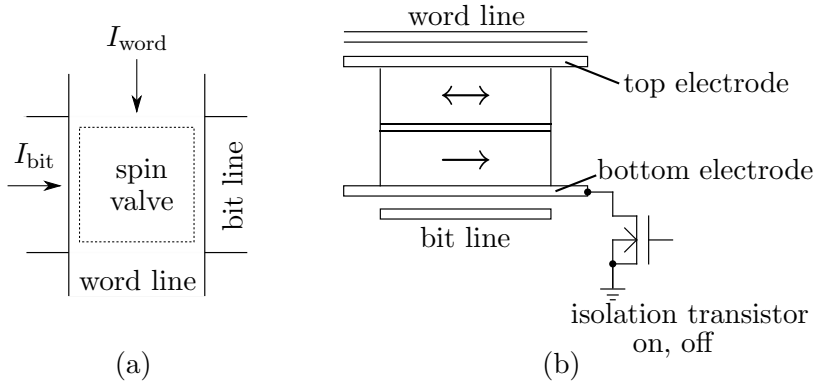


Figure 2.5: Sketch of a memory cell with a spin valve based on field-induced magnetization switching after Engel *et al.* and Slaughter [100, 151]. (a): Top view of the memory cell; the open borders of the write line and bit line indicate that the memory cells are arranged in a matrix. I_{word} is the current across the word line and I_{bit} the current across the bit line, respectively. (b): Assembly of the memory cell from the side. The isolation transistor controls the current from the top electrode to the bottom electrode. If the transistor is switched off, it possesses a high electrical resistance. It now prevents that a current on the word line can flow across the spin valve.

but not connected to the spin valve. The bit line lies underneath the spin valve, and is also not directly connected to the spin valve. The lower side of the spin valve is connected to a bottom electrode and its top face is connected to an electrode on top. The bottom electrode is connected to the drain of a field-effect transistor which controls if the spin valve is programmed (in other words if its resistance is changed or not). The transistor is called the *isolation transistor*. In the read mode the isolation transistor is switched on, which means a sensing current can flow from the word line to the isolation transistor. If the transistor is switched off, it possesses a high electrical resistance. It now prevents that a current on the word line can flow across the spin valve. For a reliable operation it is important that the resistance of the spin valves is not changed unintentionally. This implies a certain minimal

distance between adjacent cells at a specified current on word and bit line. Maffitt *et al.* review the design of field-driven spin valves in detail [152].

Current-driven switching

In 1996 Slonczewski predicted that a spin-polarized current changes the magnetization of a layer in the spin valve. Slonczewski assumed that the current flows perpendicularly to the ground plane of the spin valve, as indicated in Fig. 2.4 [153]. Electrons get spin-polarized when they traverse through the fixed layer. Their spin orientation depends on the magnetization in that layer. Electrons with spins that are aligned opposite to the localized spins in the fixed layer are reflected at the interface of that layer. A current traversing from the fixed layer to the free layer exerts a torque on the magnetization of the free layer that tends to align its magnetization parallel to the one of the fixed layer. On the other hand, a current flowing in the opposite direction causes an antiparallel alignment [66]. The torque of the itinerant electrons on the magnetization is called the spin-transfer torque (STT) in magnetic multilayers. The advantage of STT-driven spin valves would be an increase of the density of devices per unit area compared to field-driven spin valves. Now practically no magnetic field would be involved in switching the resistance of a spin valve. The mechanism has been observed in several experiments [147, 154].

For spin valves with a tunneling barrier between both ferromagnetic layers Slonczewski's theory is directly applicable. Parkin *et al.* explain however that the magnitude of the tunneling magnetoresistance effect is closely related to the degree of spin polarization of the tunneling electrons. The higher the spin polarization is, the higher the resistance change is [155]. Thus the situation where the spacer layer is a tunneling barrier is very similar to that where the spacer is a non-magnetic metal. Frequently the term spin-transfer torque is used also for spin valves with tunneling barriers [96].

Thermally assisted switching

If a ferromagnet is heated up above a material-dependent temperature, the so-called *Curie temperature*, the spontaneous magnetization in the sample vanishes [50]. The idea behind thermally assisted switching is to heat up the ferromagnetic layer that couples with an antiferromagnetic layer above a blocking temperature. In turn the orientation of the antiferromagnetic layer is set while cooling the layer to room temperature by applying a magnetic field. Prejbeanu *et al.* describe this mechanism in greater detail. They demonstrate that a current pulse of 500 ps was sufficient to switch the fixed layer [156].

2.5 Modeling and simulation of spin valves

As described in Sec. 2.3, spin valves will become important for future computing systems. Over the years the complexity of computing systems has drastically been increased by their designers. Designs that consist of 10^5 up to 10^7 components are know as VLSI designs. VLSI stands for *very-large scale integration* [157]. To handle the complexity of a VLSI design Gajski and Kuhn proposed the so-called *Y chart* [158], which is shown in Fig. 2.6[4]. According to Gajski and Kuhn, a system can be described in three different domains, its behavioral representation, its structural representation, and its geometrical representation. All representations can be considered at different levels of abstraction. Each level is indicated by a concentrical circle in Fig. 2.6. In order to explain the different representations of a system, Gajski and Kuhn give the example of an XOR gate. If the inputs of the gate are denoted as a and b and the output as x, the XOR function is given as

$$x = \bar{a} \cdot b + a \cdot \bar{b}.$$

The representations are shown in Fig. 2.7. Similar flow charts between different levels of abstraction were proposed by various authors [160–163]. For each level of abstraction in the Y chart, there are tools available for system design. The higher the level of abstraction, the less detailed a system is described. This is particularly useful, because abstraction helps to cope with the complexity.

The basic level for the system design is the *circuit level*. The behavior of each component or device of the circuit is described by its electrical properties, that is, the *U-I* characteristic. The interplay between the components is expressed by Kirchhoff's laws [164]. The electrical properties of a component are expressed in terms of its model, more commonly referred to as the *device model*:

- The behavior of an Ohmic resistor in its simplest form is given in SPICE by

  `RXXXXXX n+ n- value`,

  where `XXXXXX` is an alpha-numeric string for naming, `n+` and `n-` are the element nodes, and finally `value` is the value of the electrical resistance in Ω. In SPICE there is also a more sophisticated resistor model that allows for the calculation of the resistance based on geometric information and to be corrected for temperature [165]. Ohm's law $R = U \cdot I$ describes the $U - I$ characteristic of a resistor, where U is the applied voltage, and I is the current flowing through the resistor R.

- A plate capacitor is described by the model

  $$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d},$$

[4] A recent processor from Intel consists of approximately 1.72 billion transistors [16]. This is an *ultra-large scale integration* (ULSI) design [159]. The universality of the Y chart though is not discussed in this work.

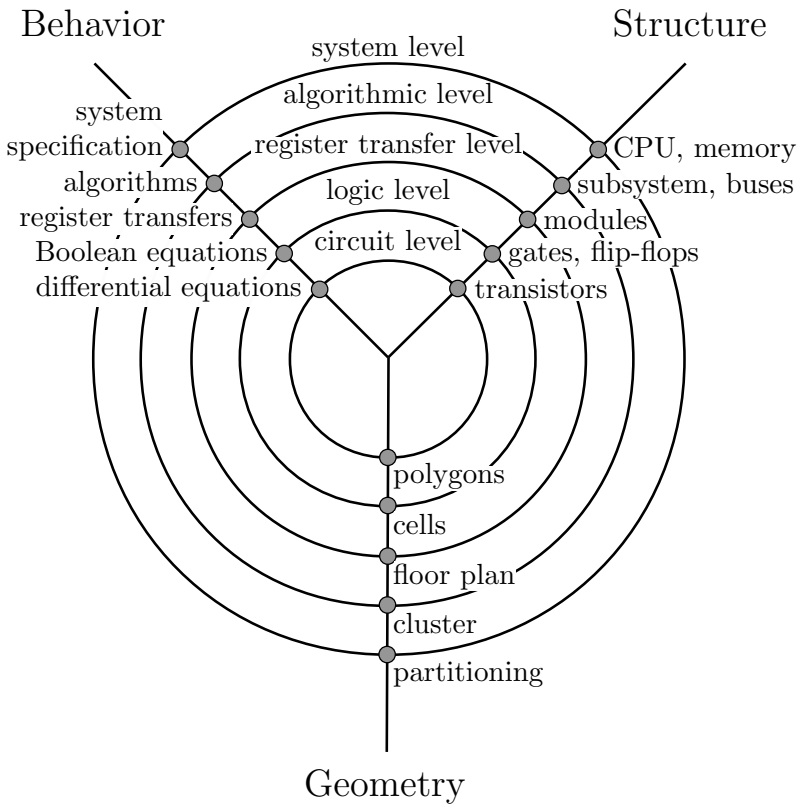


Figure 2.6: Y chart after Gajski and Kuhn [158]. A system can be described in three different domains, the behavioral representation, the structural representation, and the geometrical representation. The circles represent different levels of abstraction. The innermost circle represents the lowest level of abstraction and the outermost circle denotes the highest level of abstraction. The behavioral representation describes the functionality of the system, its inputs and outputs. Here it is important *what* the system is supposed to do, not *how* the functionality is achieved. The geometrical representation describes the geometry of the system; Of particular interest in this domain is *where* components are placed, e.g. a floor plan of the system or the wiring between the system's components. In the structural representation the structure of the system is described.

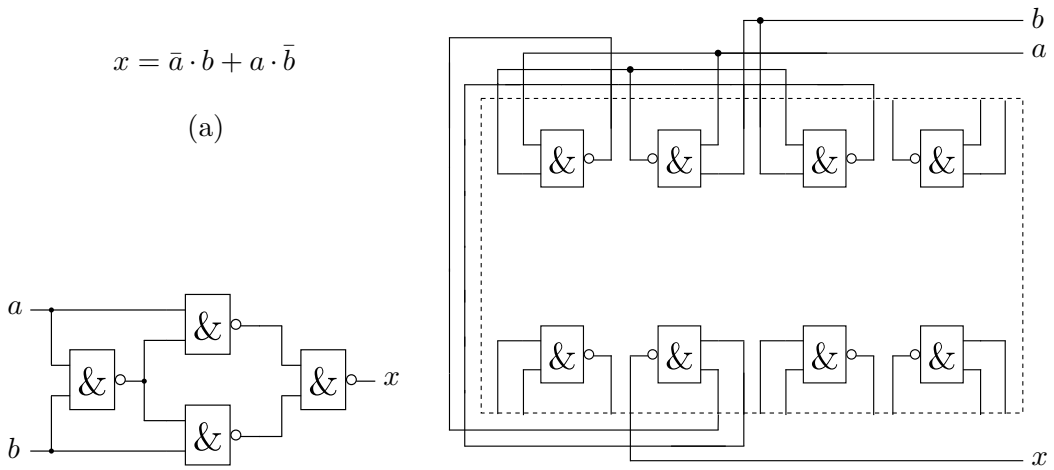


Figure 2.7: Example for the Y chart: different representations of an XOR function with two inputs. (a): a functional representation in terms of a Boolean equation, (b): a structural representation, and (c): a geometrical representation where every gate of the structural representation is assigned to a physical location. The dashed line indicates the housing of the respective integrated circuit.

where C is the capacitance in F, $\varepsilon_0 = 8.8541 \cdot 10^{-12}$ F/m is the dielectric constant in vacuum, ε_r is the material-dependent dimensionless relative permittivity, A is the area of the plates in m^2, and d is the distance between the plates in m [166]. For a capacitor holds $I = C \cdot \frac{dU}{dt}$, where I is the current in A, U is the voltage over the capacitor in V, and t is the time in s [164].

- According to the Shockley equation, the forward current of a diode I_D can be calculated by

$$I_D = I_S\left(\exp(\frac{U_D}{U_T}) - 1\right),$$

where I_S is the reverse bias saturation current, U_D is the voltage over the diode, and $U_T = \frac{k_B \cdot T}{e}$ is the temperature voltage [167]. k_B is the Boltzmann constant, T is the ambient temperature and e is the elementary charge.

The accuracy of the results with respect to experimental references essentially depends on the quality of the underlying model. It is clear that the Shockley equation cannot yield the most accurate and predictive results for the current through a diode. In this model the only difference between any two diodes is their reverse bias saturation current; the temperature voltage U_T only depends on the ambient temperature. For reliable results more complex models must be used that account for all relevant phenomena. On the other hand, a complex model may lead to time-consuming calculations. The trade-off between accuracy and the

complexity of the computation the model is a so-called *compact model* [168–171]. Verret identifies quality criteria for a compact model [172]:

- A quality model captures all relevant effects in the device. If available the results should match with experimental data.
- It is predictive at a sufficient accuracy. The model allows one to gain knowledge of the physics of the device.
- The model does not contain integrals, differentials or derivatives.
- A compact model should demonstrate a novel method or approach to increase the efficiency of the simulation without loss of accuracy.
- The model provides new insights into the function, performance characteristics, or limits of conventional devices and ideally even suggests means of improvement for the device.

A well-known compact model for field-effect transistors is the Shichman-Hodges model. It is an equivalent circuit mimicking the $U - I$ characteristics of a field-effect transistor based on the work of Ihantola and Moll [173, 174]. Ebers and Moll proposed an equivalent circuit mimicking a bipolar transistor [175]. In 2003 Laffont *et al.* published a compact model for Flash memory devices [176]. A compact model for a field-effect transistor made of carbon nanotubes was recently published by Frégonèse *et al.* [177].

In order to study the feasibility of spin valves in reconfigurable logic devices, what system designers need is a compact description of the behavior of a spin valve with emphasis on the electrical characteristics[5]. The magnetization dynamics of a spin valve is usually modeled by the micromagnetic model [141–145]. It allows to spatially resolve the dynamics of the magnetization in the free layer of a spin valve. In order to reduce the complexity, the spatial resolution can be reduced. The reduction results in the *macrospin model*. Here the dynamics in each layer is frozen out, such that it can be treated as one single spin. Such a coarsening is crucial since it reduces the accuracy of the micromagnetic model with respect to actual spin valves [146]. The validity of the macrospin model is still under debate. An important issue concerning the micromagnetic model is that not all relevant electrical properties of a spin valve, e.g. the electrical resistance of a spin valve, can directly be extracted from the simulation without additional calculations.

Compact models for spin valves – State of the art

The micromagnetic model is thus not the appropriate choice for simulating large arrays of spin valves. Instead, a compact description is required. In the literature two categories of compact models for spin valves are dominant. The first category of compact models can be denoted as *phenomenological models*. Their accuracy can be tuned to experimental reference data. The original spin valve is considered to be a black-box system; the origins of the spin

[5] This includes spin valves in memory cells.

valve's behavior are unknown or irrelevant. In 1998 Das and Black proposed an electrical circuit mimicking the hysteresis of a spin valve using the commercial simulation program HSPICE [3, 178]. This program is an electronics simulator. Based on experimental data, the hysteresis was expressed with a non-inverting Schmitt trigger and two piecewise linear voltage sources. The output voltage of the Schmitt trigger showed a rectangular-shaped hysteresis which attained two levels. The hysteresis was split into two branches, an upper and a lower branch. The actual output voltage was expressed through one of the piecewise linear voltage sources. Subsequently, the authors extended the functionality of their circuit by modeling the thermal behavior of a spin valve [179]. Das and Black employed an ideal operational amplifier in their circuit. There are two advantages of also using an electronics simulator:

1. It is quite convenient to include additional circuitry. A field-effect transistor could serve as a current source to switch the magnetization of the spin valve.

2. The hysteresis of a spin valve can plainly be implemented with an electric circuit, the Schmitt trigger (cf. Ch. 3).

Among many different tools for circuit simulation, the simulator SPICE is probably the best-known program for this purpose [180]. There are incompatibilities between different versions or spin-offs of SPICE. Das and Black used HSPICE's ideal operational amplifier for their circuit; in HSPICE the identifier for this device is "E". In SPICE an idealized operational amplifier does not even exist; here this identifier stands for linear voltage-controlled voltage sources [165, 180]. Furthermore SPICE lacks of controllable resistors which have been used by Das and Black in their circuit.

The problem of incompatibility between different simulation programs occurs if the circuit is modeled with devices that are not common to each program involved. It can be overcome by remodeling the respective devices or components with devices that are common to both programs. A new design is justified though if using it further reduces the complexity of the design. Depending on the application, it might be sufficient to model the resistance of a spin valve simply by Ohmic resistors or in combination with capacitors [181–183]. In 2005 Lee *et al.* proposed an equivalent circuit tailored to magnetic tunnel junctions which incorporates the temperature dependence of the hysteresis curve and the Stoner-Wohlfarth asteroid curve. The hysteresis of that circuit is assumed to be rectangular-shaped [4]. Recently the authors published an extended version of the circuit. They calculated a fitting function for the high-resistance state of the respective spin valve; the resistance in the low-resistance state was assumed to be constant [184]. Using models of real operational amplifiers leads to the problem that the simulation might not converge. The matter of convergence of a simulation within an electrical circuit for spin valves was recently addressed by Mukherjee and Kurinec [5]. Using realistic models of real devices, especially operational amplifiers, means that the spin-valve circuit inherits the characteristics of the devices used. This affects for example the range of the input signal for the spin valve; for details cf. Sec. 3.1.

Besides equivalent circuits that mimic the behavior, there is another category of compact

models for spin valves. The second category can be denoted as *analytical models*. Here the electrical characteristics of a spin valve are not approximated by an equivalent electrical circuit. Instead of describing the behavior of a spin valve indirectly with circuits like a Schmitt trigger, the core of an analytical model is a physical model that is intended to describe the relevant properties of the spin valve. The validity of such a physical model is the most crucial aspect of an analytical compact models, because its validity determines the accuracy of the compact model compared to experimental data. A first example for an analytical model was published by Csaba *et al.* in 2003. The energy of an inductor is used to express the magnetization for circular ferromagnetic dots. Following this approach, the mutual influence of neighboring dots was expressed with coupled inductors [185]. The circuit can be simulated with programs like SPICE. The computation of the spin-transfer torque and exchange field for spin valves based on Csaba's proposal was performed by Malathi and Prabhakar [186,187].

For the purpose of a logic or memory device, the key property of a spin valve is its electrical resistance which can be controlled with either a magnetic field or an electrical current. Kammerer *et al.* describe the modeling of a magnetic tunnel junction (this is a spin valve where the spacer layer is an insulator) in VHDL[6] using Jullière's model for the conductance of a tunnel barrier that depends on the applied voltage. The Stoner-Wohlfarth model for the hysteresis was also included [188]. In the same year, a magnetic tunnel junction with a difference in the resistance of both states of almost 103 % was presented. The experiment was simulated in SPICE using Jullière's model [189]. The simulation is not reproducible, because the article lacks the suitable description of the circuit. An implementation of Jullière's model was written in the programming language C by Prenat et al. [190]. Later Slonczewski's model for the spin-transfer torque in a spin valve was included [191].

In 1963 Simmons published an article on tunneling through a thin insulating film. Based on Simmons' work there exists a number of compact models for magnetic tunnel junctions. These are either hardly reproducible, because some parts of the implementation of the model are left out [192, 193] or are written in HSPICE [194]. A third model for the conductance of a thin oxide layer has been developed by Brinkman. It was suggested by Zhao *et al.* to combine Brinkman's model of the conductance of a thin insulating layer and Slonczewski's model of the spin-transfer torque [195]. This model was implemented in Verilog, which is another high-level hardware description language.

All models related to the second category include a description of the conductance of an insulating spacer layer between free and fixed layer of a spin valve. For spacer layers composed of a metal, these analytical models are not applicable. Literature research did not yield any proposal on a compact model for spin valves using Slonczewski's model.

[6] VHDL is a high-level hardware description language.

Chapter 3

Compact models for spin valves

In this chapter two different approaches for the compact model of a spin valve are described. Both models are expressed in terms of electrical circuits. As Sec. 2.5 on page 31 et seqq. shows this is not the only approach for compact models of spin valves. Using an equivalent electrical circuit however is particularly useful. An electrical circuit mimicking a spin valve allows simulating directly the combination of the spin valve with other devices. Whether a current-driven or a field-driven spin valve is to be imitated, always an electrical current has got to be generated. A field-effect transistor operated in saturation generates an almost constant direct current. Apparently a field-effect transistor is a simple means to drive a spin valves. An equivalent electrical circuit makes the spin valve accessible to engineers, because it describes its behavior in the language of a circuit designer. A prominent example of an equivalent electrical circuit as a compact model is the Shichman-Hodges model for field-effect transistors [173].

The work "Spin Valves For Innovative Computing Devices And Architectures" was presented at the 2008 Summer Computer Simulation Conference SCSC'08 (June 16-19, 2008, Edinburgh, United Kingdom) (Ref. [196]). In this paper the concept of a circuit is described, which mimics a spin valve whose resistance shows a rectangular-shaped hysteresis. In Sec. 3.1 on page 36 et seqq. the final version of the circuit and its dimensioning to a given spin valve are depicted by means of two case studies. The first case study shows the customization of the circuit to a spin valve with a comparatively small difference between the resistances for the states of the spin valve. The second case study deals with the dimensioning of the circuit for a spin valve with a higher difference between the resistances for both states. It is evaluated whether or not the circuit matches the criteria for compact models (cf. Sec. 2.5). The feasibility of logic gates is examined by picking up the former two case studies. Section 3.3 depicts an equivalent circuit whose accuracy can be tuned with respect to experimental data. Although different in their assembly, both circuits express the resistance of a spin valve through the corresponding voltage drop.

3.1 Compact model for a spin valve with an idealized hysteresis

Since the publication of the article [196] in 2008 extensions of the circuit have been developed. In particular dimensioning of the circuit is a major advance. The following section introduces the design of the new circuit. It can be shown that the circuit can conveniently be adopted to a spin valve's hysteresis.

Motivation

The presented circuit is intended to be a simple and flexible means to make spin valves accessible to systems engineering. In particular the simplicity of the circuit is important when the circuit is supposed to be used for complex designs using a large number of spin valves. As explained in Sec. 2.5 an equivalent electrical circuit is beneficial for a compact description of a spin valve's behavior. The article "Spin Valves For Innovative Computing Devices And Architectures" describes the concept of a circuit that allows simulation of a spin valve whose resistance is a rectangular-shaped hysteresis. A rectangular hysteresis can be considered as the first approximation of a realistic hysteresis curve, but the circuit itself is very simple and helps estimating the feasibility of a spin valve in a logic gate or a memory cell. Using an electric circuit simulator for the analysis of a spin valve makes it possible to simulate the combination of spin valves with any electronic device. In the presented equivalent circuit the hysteresis of the spin valve is modeled with an electronic analog where the resistance of the spin valve is expressed with a transistor switch. The spin valve is modeled as a device with three terminals[1]. The transistor's state depends on a control voltage which is in turn coupled with the state of the hysteresis signal. In the following section the overall design is described, first the component responsible for the hysteresis of the control signal and second the resistance switch whose state depends on the state of the control signal. This chapter embeds two case studies: Two spin valves, one with a small and one with a large difference between both resistance states are modeled with the equivalent circuit.

Implementation of the hysteresis

The Schmitt trigger was invented by the American engineer Otto Schmitt in 1938 using two coupled tube amplifiers [197]. Today a Schmitt trigger can conveniently be set up with an operational amplifier. The Schmitt trigger is a comparator with two different thresholds or switching points. If an operational amplifier is used, the switching points are determined by two external resistors and the supply voltages. For the design of the circuit a voltage amplifier was used that amplifies the voltage difference between the inverting and non-inverting input. It is well suited for implementing a Schmitt trigger, due to its high input and low output

[1] A spin valve can be also considered as a device with two terminals. The structure of the circuit however suggests a three-terminal structure for the spin valve, comparable with a potentiometer. The circuit can be transformed into a two-terminal device by shorting two terminals.

resistance, and its high open loop gain[2]. Because of its high open-loop gain an operational amplifier acts as a comparator without negative feedback. The maximum or minimum voltage at the output stage of the amplifier is determined by the positive or negative supply voltage. A well-known example of an operational amplifier is the LM741, fabricated by National Semiconductor [198]. According to the data sheet this amplifier possesses an open-loop gain of 106.02 dB. A difference between both inputs of only +1 mV would cause an output voltage of 200 V. Actually, the maximum output voltage would be the positive supply voltage. A small negative difference of both inputs causes an output voltage equal to the negative supply voltage in contrast.

In the new design an inverting Schmitt trigger is used. The transistor's state is controlled with the output voltage of the Schmitt trigger. Every time the signal is at its high level the transistor switches on. Eventually the voltage drop (that corresponds to the resistance) over the transistor would be less than if the transistor is switched off. The simplest way to avoid this is inverting the hysteresis with an inverting Schmitt trigger. The approximation of an experimental hysteresis with a rectangular shape is justified by the following assumptions, which are valid for the experimental hysteresis of a spin valve's resistance:

1. There exist two resistance levels R_L and R_H with $R_L < R_H$; R_L is the low resistance level and R_H is the high resistance level.
2. There is one switching point S_+ to switch from R_L to R_H
3. There is one switching point S_- to switch from R_H to R_L
4. $S_+ > S_-$

The input signal may be a current which is applied to the spin valve (e.g. for current-driven spin valves). For the circuit the input signal is mapped onto an input voltage and the resistance of the spin valve is expressed in terms of an output voltage. It is assumed that 1 mA in the measurement corresponds to 1 V in the simulation[3]. If the output voltage should represent the resistance of the transistor the hysteresis has to be inverted because the transistor itself will also invert the output voltage of the spin valve circuit (see above). As a consequence the original switching point S_+ becomes S_- and S_- now becomes S_+. This is the inversion of the third assumption given above. The input voltage is denoted as U_{in}, the output voltage as U_{out}, the positive supply voltage as U_+, and the negative supply voltage as U_-. The resulting circuit is shown in Fig. 3.1, the netlist can be found in appendix A.1. The voltage at the node i is called U_i. It is fed back to the non-inverting input,

$$U_i = \frac{R_2}{R_1 + R_2} \cdot U_H. \tag{3.1}$$

[2]These properties are demanded from (voltage) operational amplifiers. A high input resistance is desired in order to prevent high input currents. A low output resistance is necessary to avoid unwanted loads to subsequent devices. These requirements can be fulfilled with a multistage amplifier. The situation for voltage amplifiers is different than for transconductance amplifiers, transimpedance amplifiers or current amplifiers.

[3]A conversion of an electrical current to a voltage can be achieved with an operational amplifier [199]. For the simulation the conversion can be performed by a current-controlled voltage source; see also the netlist in appendix A.6.

The factor $\frac{R_2}{R_1+R_2}$ must satisfy

$$\frac{R_2}{R_1+R_2} = \frac{U_{\text{in,off}}}{U_+} = \frac{U_{\text{in,on}}}{U_-}, \tag{3.2}$$

where $U_{\text{in,off}}$ corresponds to S_- and $U_{\text{in,on}}$ corresponds to S_+. If the resistors are chosen first, this might lead to a small value for U_+, which is not a good decision, since the supply voltages determine the range of reliable operation of the amplifier. Input voltages should be less than U_+ and greater than U_-. Instead U_+ should be chosen first.

Implementation of the resistance switch

The resistance of the spin valve is assumed to be either at a high or a low level, R_{AP} or R_P respectively. Both resistances correspond to either parallel or anti-parallel alignment of the magnetizations in both layers of a spin valve. The equivalent circuit of the spin valve is shown in Fig. 3.1, the netlist can be found in appendix A.1. The effective resistance of the spin valve is expressed through the resistors R_5, R_6, and R_M which is implemented through the state of the transistor. In the circuit an n-channel field-effect transistor in enhancement mode is used. The output voltage U_H of the Schmitt trigger is the gate-source voltage of the transistor. It can attain two values, U_+ or U_-. If $U_H = U_+$ holds, the transistor is switched on and R_M is at its low level R_A. Consequently, in the case of $U_H = U_-$ the transistor is switched off and R_M is at its high level R_B. For the low resistance of the spin valve R_P this yields

$$\frac{1}{R_P} = \frac{1}{R_A + R_5} + \frac{1}{R_6}. \tag{3.3}$$

A similar expression can derived for $\frac{1}{R_{AP}}$ (R_{AP} denotes the high resistance of the spin valve). It follows from Eq. 3.3 for R_P

$$R_P = \frac{R_6 \cdot \big(R_A + R_5\big)}{R_5 + R_6 + R_A}. \tag{3.4}$$

Similarly the equation for R_{AP} can be derived from Eq. 3.3 by replacing R_A with R_B. Finally

$$\frac{R_P R_5 + R_P R_A}{R_A + R_5 - R_P} = \frac{R_{AP} R_5 + R_{AP} R_B}{R_B + R_5 - R_{AP}}. \tag{3.5}$$

Resolving this equation yields a quadratic equation [200]

$$ax^2 + bx + c = 0, \tag{3.6}$$

where

$$a = R_P - R_{AP} \tag{3.7}$$

$$b = R_P \cdot \big(R_A + R_B\big) - R_{AP} \cdot \big(R_A + R_B\big) \tag{3.8}$$

$$c = R_P \cdot \big(R_A R_B - R_A R_{AP}\big) - R_{AP} \cdot \big(R_A R_B - R_B R_P\big). \tag{3.9}$$

In order to determine R_5 and R_6 the resistance of the transistor M_1 has to be calculated. If M_1 is operated in the Ohmic mode it can be used as a controllable resistor. As a precondition

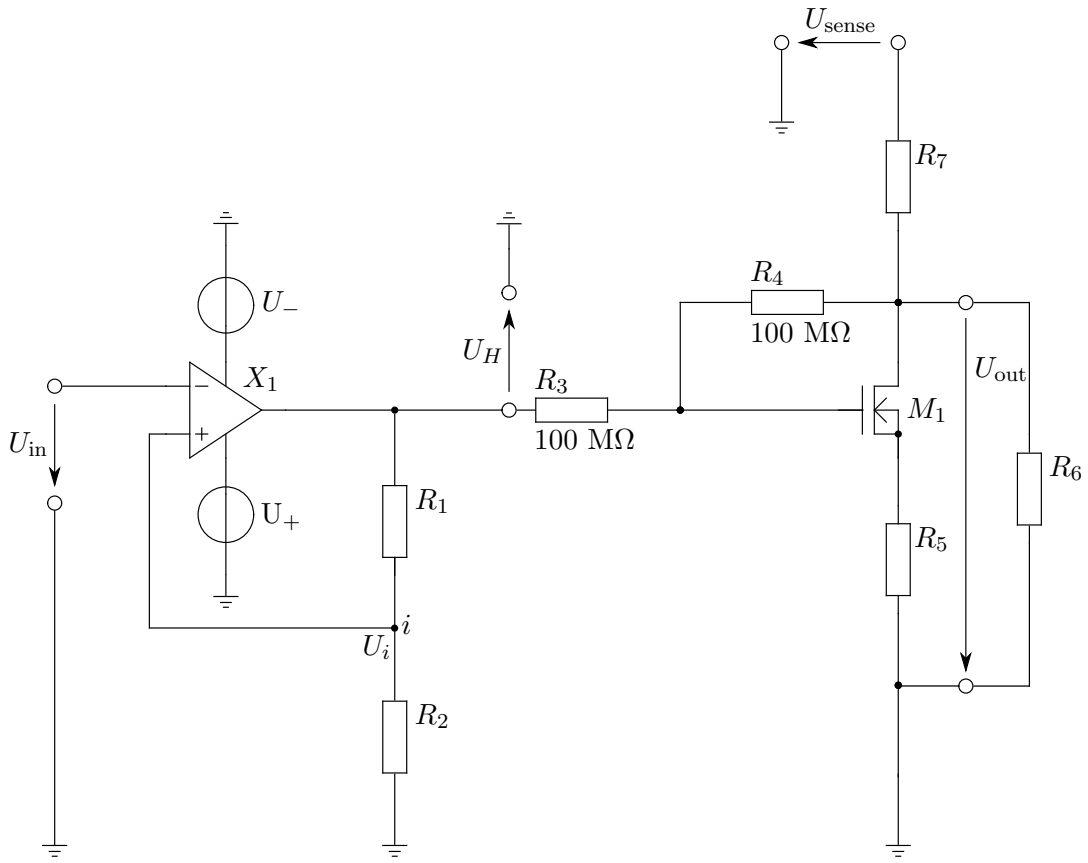


Figure 3.1: Circuit diagram of the equivalent circuit for the idealized rectangular hysteresis of a spin valve's resistance in terms of the output voltage U_{out}. U_{in} is the input voltage. The operational amplifier X_1 is an inverting Schmitt trigger with the resistors R_1 and R_2. The voltage U_i is fed back to the non-inverting input of X_1. R_3 and R_4 linearize the resistance of the n-channel field-effect transistor M_1 in the Ohmic mode. Together with the resistors R_5 and R_6 M_1 mimics the effective resistance of the circuit which is either high or low. The effective resistance of the circuit forms a voltage divider with the external resistor R_7. A sensing voltage U_{sense} can be applied to measure the resistance of the spin-valve circuit. The netlist can be found in appendix A.1.

R_3 and R_4 have a high resistance value (in the order of some MΩ) [201][4]. If $R_3 = R_4$, the resistance of the transistor in the Ohmic mode is given by

$$R(U_H) = \frac{1}{K \cdot \left(\frac{U_H}{2} - U_{\text{th}}\right)}, \tag{3.10}$$

where U_{th} is the threshold voltage and K is the transconductance parameter of the transistor. The transistor is operated in the Ohmic mode if $U_{GS} \geq U_{\text{th}}$ and $0 \leq U_{DS} < U_{GS} - U_{\text{th}}$, where U_{GS} is the transistor's gate-source voltage and U_{DS} is the applied voltage between drain and source.

A convenient method to determine the resistance of a transistor when it is switched off is using a Wheatstone bridge [202]. The circuit is shown in Fig. 3.2. The netlist can be found in appendix A.2.

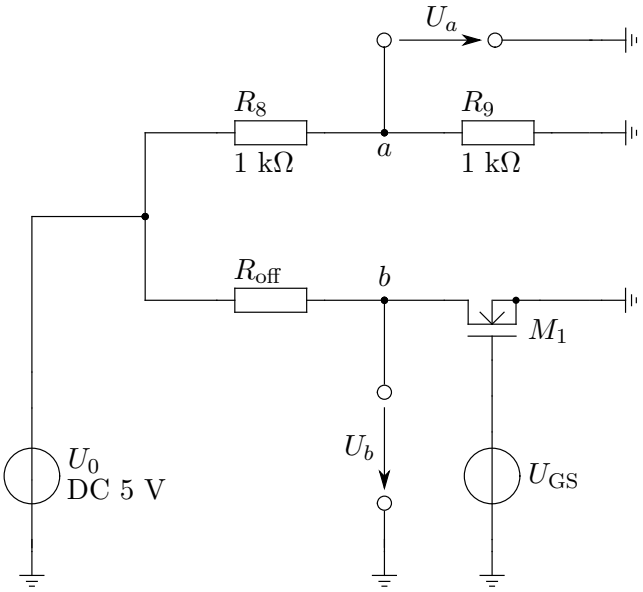


Figure 3.2: Circuit diagram of a Wheatstone bridge for the measurement of the resistance of the n-channel field-effect transistor M_1. The resistors R_8 and R_9 are fixed. The input voltage U_0 is split up over both resistors at the ratio of their resistances. U_a is the voltage drop over R_9. The resistor R_{off} is set such that U_b matches U_a. If this condition is satisfied, the transistor's resistance and R_{off} have the same ratio as R_8 and R_9. The transistor M_1 is off at the given gate-source voltage U_{GS} (cf. the case studies in Sec. 3.1 for details). The netlist can be found in appendix A.2.

[4]The resistors R_3 and R_4 linearize the resistance of the transistor when it is operated in the Ohmic mode. Both resistors must have resistances in the order of some MΩ in order to prevent the drain-source current flowing elsewhere than from the drain terminal to the source terminal.

Case study 1: Spin valve with low resistance lift

Dimensioning the circuit requires reference data. The choice in this case study is the experimentally measured hysteresis curve in the work of Albert *et al.* [147], which is interesting for two reasons (i) this work demonstrates the switching of a spin valve's resistance through spin-transfer torque that may be the dominant mechanism for switching in the future and (ii) the difference between both states, that is, the difference between high and low resistance is approximately 0.05 Ω. The authors measured the differential resistance dV/dI. In order to determine the electrical resistance, first dV/dI (the symbol V has been used by Albert *et al.* for naming voltages) has got to be integrated with respect to I. Integration yields the voltage over the spin valve. The ratio V/I is the electrical resistance. The resistance of the spin valve can be explained with the giant magnetoresistance effect. The authors developed a cobalt/copper/cobalt pillar (cf. Fig. 3.3). They performed two sweeps of the current and measured the resulting differential resistance. When the current is swept from −12 mA to +12 mA the differential resistance switches from low level to high level at a current of +1.7 mA. During the sweep from +12 mA to −12 mA the differential resistance switches from its high value to its low value at a current of −4.3 mA. The assembly of the spin valve is shown in Fig. 3.3. The resistance that corresponds to the parallel orientation of the magnetizations in the spin valve (meaning the magnetization in the free layer and the fixed layer) and thus to the low resistance state is assumed to be $R_P = 1.54\ \Omega$. The resistance in the antiparallel configuration of the magnetizations is assumed to be $R_{AP} = 1.59\ \Omega$[5]. This resistance corresponds to the high resistance of the spin valve. The difference is

$$\Delta R = R_{AP} - R_P = 0.0500\ \Omega. \tag{3.11}$$

Since it was assumed that an applied current of 1 mA in the experiment corresponds to an input voltage of 1 V in the circuit, S_+ lies at a voltage $U_{\text{in,on}} = -4.3000$ V. The switching point S_- lies at a voltage $U_{\text{in,off}} = +1.7000$ V. If U_+ is chosen to be +10 V this corresponds to

$$\frac{R_2}{R_1 + R_2} = \frac{U_{\text{in,off}}}{U_+} = \frac{1.7000\ \text{V}}{10\ \text{V}} = 0.1700, \tag{3.12}$$

where R_1 and R_2 are the resistors of the Schmitt trigger (cf. Fig. 3.1). If R_2 is chosen to be 1 kΩ this yields

$$R_1 = 4.8823\ \text{k}\Omega. \tag{3.13}$$

Consequently, for $U_{\text{in,on}} = -4.3000$ V this results in

$$U_- = \frac{U_{\text{in,on}} \cdot \left(R_1 + R_2\right)}{R_2} = \frac{-4.3000\ \text{V} \cdot \left(4.8823\ \text{k}\Omega + 1\ \text{k}\Omega\right)}{1\ \text{k}\Omega} = -25.2939\ \text{V}. \tag{3.14}$$

The Schmitt trigger was implemented with a model of the LM8261 operational amplifier from National Semiconductor [203]. The choice of the operational amplifier depends on the spin

[5] In the original work the differential resistance was measured. For the circuit in Sec. 3.3 dV/dI was integrated (cf. page 64 et seqq.). Based on the integration V/I was computed. The values of the resistance are very close to those for the differential resistance. The assumption $R_P = 1.54\ \Omega$ and $R_{AP} = 1.59\ \Omega$ therefore still is reasonable, see also Fig. 3.28.

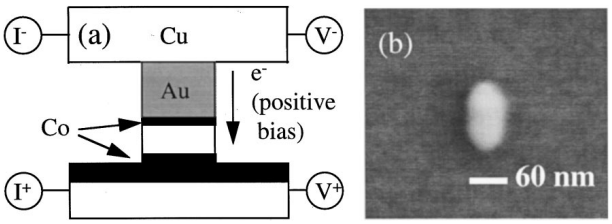


Figure 3.3: (a): Schematic cross section of the spin valve for the first case study. A copper layer with a thickness of 80 nm at the bottom serves as an electrode. The spin valve consists of a cobalt layer of 40 nm as the fixed layer next to the bottom electrode. The spacer layer is 6 nm thick and made of copper. The free layer again is a cobalt layer with a thickness of 2.5 nm. (b): Scanning electron micrograph of the spin valve before it was coated with the gold layer. The area of the spin valve is approximately 60 nm × 130 nm. Reprinted with permission from Ref. [147]. Copyright 2000 American Institute of Physics.

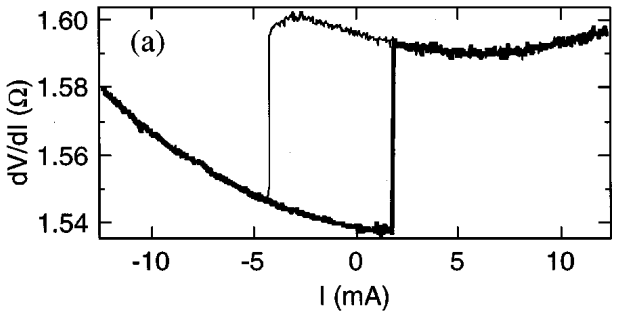


Figure 3.4: (a): Differential resistance dV/dI of the spin valve. The resistance can be calculated by integrating dV/dI with respect to I. Integration yields the voltage drop over the spin valve. The resistance is the ratio of voltage drop over the spin valve and applied current. Reprinted with permission from Ref. [147]. Copyright 2000 American Institute of Physics.

valve to be mimicked. Any other operational amplifier may be used instead of the LM8261 as long as it allows to properly mimic the switching points of the hysteresis.

The model for the transistor M_1 is the default model of SPICE, the so-called Shichman-Hodges model. In SPICE the default model is selected by the entry `LEVEL=1` within the definition of the transistor model. The default parameters were used for the transistor, except for the transconductance parameter $K = 2.2550\ \mathrm{A/V^2}$. By default, the threshold voltage at zero bias is $U_{\mathrm{th}} = 0\ \mathrm{V}$. In the current setup the resistance of the transistor in the on-state can be written as

$$R_{\mathrm{on}} = R(U_H) = \frac{1}{K \cdot \left(\frac{U_H}{2} - U_{\mathrm{th}}\right)} = \frac{1}{2.2550\ \mathrm{A/V^2} \cdot \left(\frac{10\ \mathrm{V}}{2} - 0\ \mathrm{V}\right)} = 8.8692 \cdot 10^{-2}\ \Omega. \quad (3.15)$$

The value for K was chosen in order to obtain the value for R_{on}. K and U_{th} can be modified in order to match values for real transistors as long as $R_{\mathrm{on}} \ll R_{\mathrm{off}}$ is satisfied. If $U_H = 25.2939\ \mathrm{V}$, the transistor is switched off, because the gate-source voltage is below the threshold voltage. The gate-source voltage is then given by

$$U_{GS} = \frac{U_H + U_{DS}}{2} = \frac{-25.2939\ \mathrm{V} + 2.5000\ \mathrm{mV}}{2} = -12.6457\ \mathrm{V} < U_{\mathrm{th}} = 0\ \mathrm{V}, \quad (3.16)$$

when a sensing voltage $U_{\mathrm{sense}} = 5.0000\ \mathrm{mV}$ is used (cf. Sec. 3.1). Together with the resistors R_5 and R_6, the resistance of the transistor yields a voltage at the drain terminal of $\frac{1}{2}U_{\mathrm{sense}} = 2.5000\ \mathrm{mV}$. The resistance of the transistor was determined in a Wheatstone bridge. This circuit is shown in Fig. 3.2. Simulations showed that the transistor's resistance in the given operating point is

$$R_{\mathrm{off}} \approx 0.9960\ \mathrm{T\Omega}, \quad (3.17)$$

because with this value for R_{off} the comparison of the voltage drops between the nodes a, b, and ground in the Wheatstone bridge yielded

$$\begin{aligned} U_a &= 2.50000\ \mathrm{V}, \\ U_b &= 2.50002\ \mathrm{V}. \end{aligned}$$

With the values for R_{on} and R_{off} the values for R_5 and R_6 can be determined. Both depend on the hysteresis to be mimicked. Clearly, a rule of thumb is that R_6 must be chosen

$$R_6 = R_{AP} = 1.5900\ \Omega, \quad (3.18)$$

because of the high resistance R_{off} (the resistance of resistors in parallel connection is dominated by the resistor with the smallest resistance). For R_5 this results

$$R_5 \approx 48.8612\ \Omega. \quad (3.19)$$

Figure 3.5 shows the hysteresis curve of the equivalent circuit for a given sensing voltage $U_{\mathrm{sense}} = 5\ \mathrm{mV}$ and the resistors $R_7 = R_{AP} = 1.5900\ \Omega$[6]. The resistance of the spin valve

[6]The value of R_7 can be chosen arbitrarily. It forms a voltage divider with the spin valve. For simplicity in the case study it was chosen to be equal to R_{AP}. In this situation half of the sensing voltage drops over the spin valve if the spin valve is set to R_{AP}.

corresponds to an output voltage

$$U_{\text{out}} = \begin{cases} \frac{R_{AP}}{R_{AP}+R_7} \cdot U_{\text{sense}} = \frac{1.5900\ \Omega}{1.5900\ \Omega+1.5900\ \Omega} \cdot 5\ \text{mV} = 2.500000\ \text{mV}. \\ \\ \frac{R_P}{R_P+R_7} \cdot U_{\text{sense}} = \frac{1.5400\ \Omega}{1.5400\ \Omega+1.5900\ \Omega} \cdot 5\ \text{mV} = 2.460064\ \text{mV}. \end{cases} \tag{3.20}$$

Simulations of the spin-valve circuit show

$$U_{\text{out}} = \begin{cases} 2.4999\ \text{mV} & \Leftrightarrow \text{spin valve is at high resistance.} \\ \\ 2.4600\ \text{mV} & \Leftrightarrow \text{spin valve is at low resistance.} \end{cases} \tag{3.21}$$

The circuit properly performs the hysteresis of a spin valve's resistance. The circuit's flexibility is underlined by the following section, in which a spin valve is mimicked with higher resistances and a higher difference between both. The validity of these results is discussed in the summary at the end of this section.

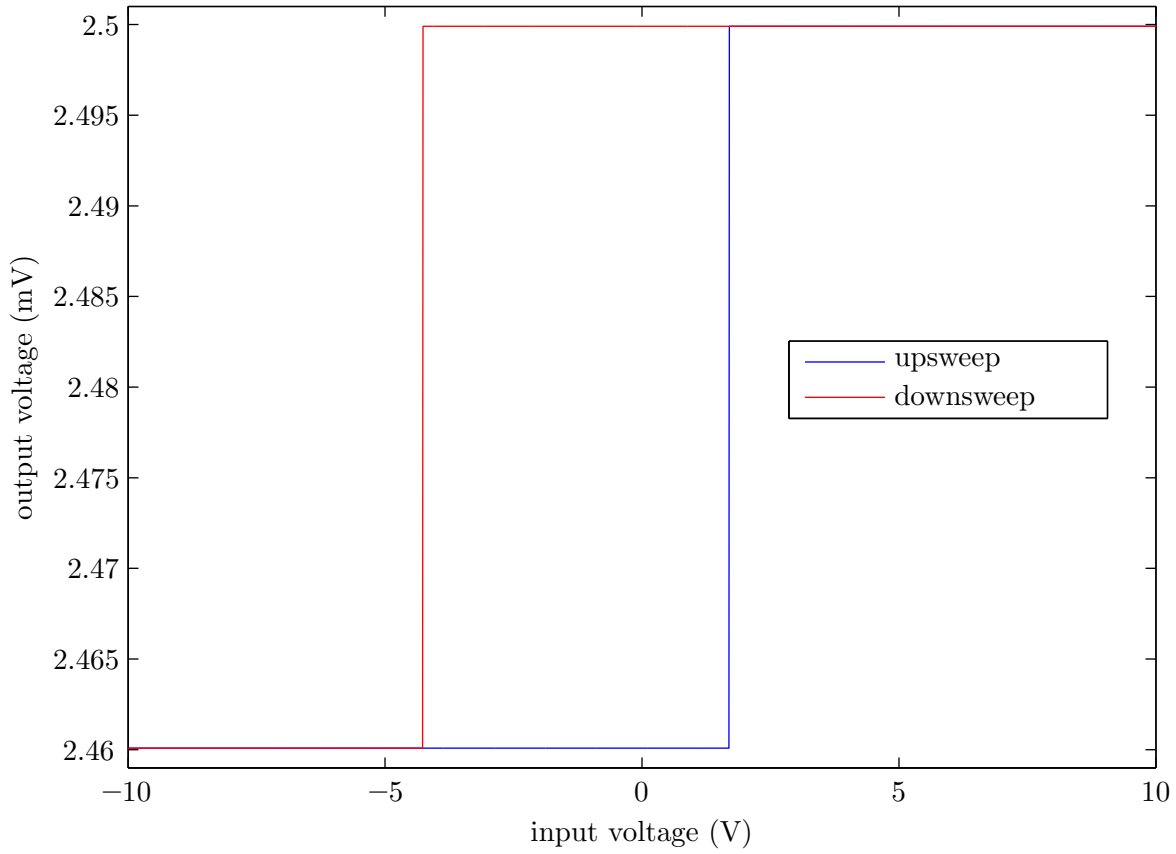


Figure 3.5: Simulated hysteresis of the output voltage of the equivalent circuit for the first case study. The upsweep of the input voltage is performed from −10 V to +10 V. The output voltage switches from the low level to the high level at an input voltage of +1.7 V. The downsweep of the input voltage is performed from +10 V to −10 V. The output voltage switches from the high level to the low level at an input voltage of −4.3 V. A sensing voltage of +5 mV was applied.

Case study 2: Spin valve with high resistance lift

In 2008 Kawahara *et al.* published an article about a 2 Mbit memory device based on current-driven spin valves [96]. The spacer layer in between the magnetic layers is made of magnesium oxide; in this case spin valves are more commonly referred to as magnetic tunnel junctions. The assembly of a memory cell including a micrograph and the $R - I$ characteristics are shown in Fig. 3.6 and Fig. 3.7. The switching of the spin valve is described by the tunneling-magnetoresistance effect. As a consequence, the difference between parallel and antiparallel orientation of the magnetization is much larger than in the first case study. Most interestingly the critical currents which are required to switch between both configurations are also much smaller than in the first case study. The hysteresis of one of the spin valves in the memory device can be approximated as

- The resistance in the parallel orientation is $R_P = 5\ \mathrm{k}\Omega$.

- The resistance in the antiparallel orientation is $R_{AP} = 7\ \mathrm{k\Omega}$.
- The spin valve's resistance switches at a current of $+200\ \mu\mathrm{A}$ from its low level to its high level. S_+ is set to 0.2 V
- The spin valve's resistance switches at a current of $-200\ \mu\mathrm{A}$ from its high level to its low level. S_- is set to -0.2 V

The supply voltages are chosen to be $U_- = -5$ V and $U_+ = 5$ V. The ratio

$$\frac{U_{\mathrm{in,on}}}{U_-} = \frac{-0.2000\ \mathrm{V}}{-5\ \mathrm{V}} = 0.0400. \tag{3.22}$$

The choice $R_2 = 1\ \mathrm{k\Omega}$ yields

$$R_1 = 24\ \mathrm{k\Omega}. \tag{3.23}$$

The same amplifier and transistor are used as in the first case study. Only the supply voltages are set differently. With these values the simulated output voltage of the Schmitt trigger is

$$U_H = \begin{cases} +4.967886\ \mathrm{V} & \Leftrightarrow \text{spin valve is at low resistance.} \\ \\ -4.959014\ \mathrm{V} & \Leftrightarrow \text{spin valve is at high resistance.} \end{cases} \tag{3.24}$$

Using Eq. 3.10 the resistance of the transistor in its on-state amounts to

$$R_{\mathrm{on}} \approx 0.1785\ \Omega. \tag{3.25}$$

If $U_H = -4.959014$ V the transistor is switched off. The resulting gate-source voltage is

$$U_{GS} = \frac{U_H + U_{DS}}{2} = \frac{-4.959014\ \mathrm{V} + 2.5000\ \mathrm{mV}}{2} \approx -2.4783\ \mathrm{V} < U_{\mathrm{th}} = 0\ \mathrm{V}. \tag{3.26}$$

Using the Wheatstone bridge it is found that for $U_{GS} = -2.4783$ V the resistance of the transistor is

$$R_{\mathrm{off}} \approx 0.9960\ \mathrm{T\Omega}. \tag{3.27}$$

A comparison of the voltage drops at the nodes a and b in the Wheatstone bridge yields

$$\begin{aligned} U_a &= 2.50000\ \mathrm{V}, \\ U_b &= 2.50002\ \mathrm{V} \end{aligned}$$

(see also Fig. 3.2). Based on the resistances of the transistor, the resistor R_5 is dimensioned as

$$R_5 \approx 17.4997\ \mathrm{k\Omega} \tag{3.28}$$

using Eq. 3.5. As expected

$$R_6 = R_{AP} = 7\ \mathrm{k\Omega}. \tag{3.29}$$

Figure 3.8 shows the hysteresis curve. In order to check if the resistance of the spin-valve

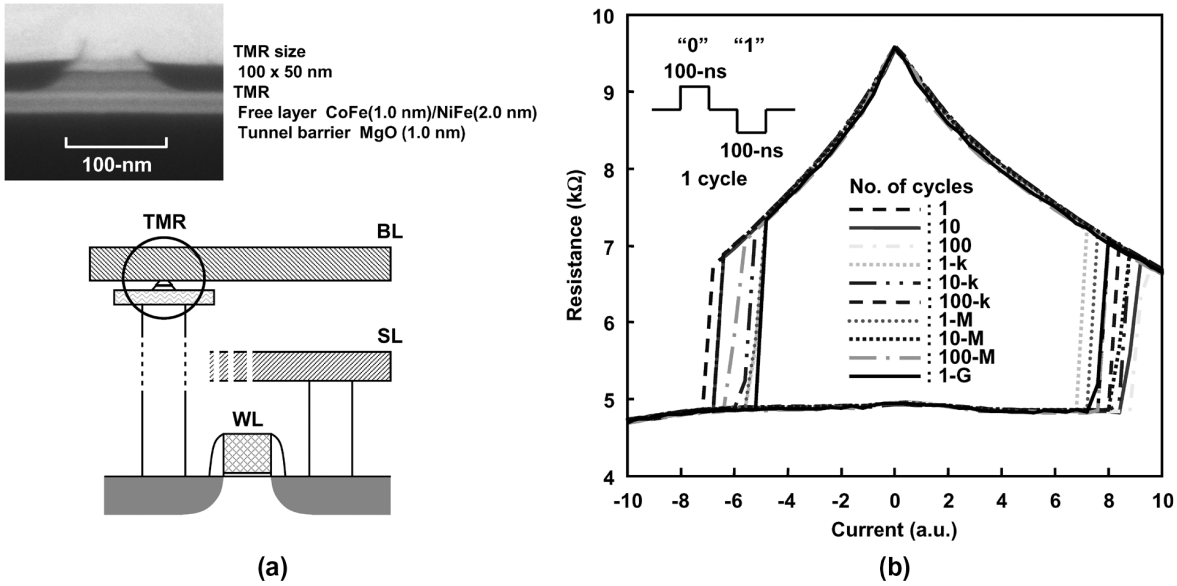


Figure 3.6: (a): The assembly of a memory cell including a micrograph (b): the $R - I$ characteristics of a spin valve for the second case study. Reprinted with permission from Ref. [96]. Copyright 2008 IEEE.

TABLE I
CHIP FEATURES

Density		2 Mb
Process		0.2-um CMOS, 1 poly, 4 metal
Memory cell size		1.6 x 1.6 um (designed under 0.4-um upper metal L/S)
Power supply		1.8 V
Write	Cell Current	200 uA
	Time	100 ns
Read	Time	40 ns
Chip module size		5.32 x 2.50 mm

Figure 3.7: Measured features of the memory chip by Kawahara *et al.*. Reprinted with permission from Ref. [96]. Copyright 2008 IEEE.

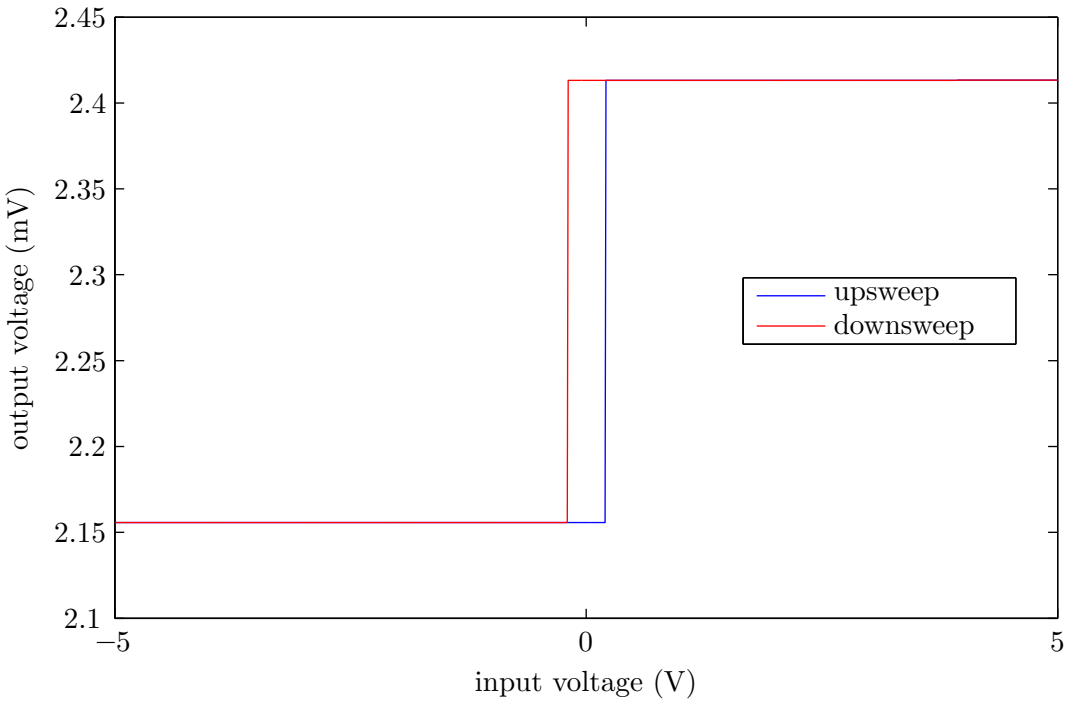


Figure 3.8: Simulated hysteresis of the output voltage of the equivalent circuit for the second case study. The upsweep of the input voltage is performed from −5 V to +5 V. The output voltage switches from the low level to the high level at an input voltage of +0.2 V. The downsweep of the input voltage is performed from +5 V to −5 V. The output voltage switches from the high level to the low level at an input voltage of −0.2 V. A sensing voltage of +5 mV was applied.

circuit is set correctly, the resistor R_7[7] is set to

$$R_7 = R_{AP} = 7\ \text{k}\Omega. \tag{3.30}$$

In this situation half of the sensing voltage $U_{\text{sense}} = 5$ mV drops over the spin valve. With the value the expected output voltage becomes

$$U_{\text{out}} = \begin{cases} \frac{R_{AP}}{R_{AP}+R_7} \cdot U_{\text{sense}} = \frac{7\ \text{k}\Omega}{7\ \text{k}\Omega+7\ \text{k}\Omega} \cdot 5\ \text{mV} = 2.5000\ \text{mV}. \\ \\ \frac{R_P}{R_P+R_7} \cdot U_{\text{sense}} = \frac{5\ \text{k}\Omega}{5\ \text{k}\Omega+7\ \text{k}\Omega} \cdot 5\ \text{mV} = 2.0833\ \text{mV}. \end{cases} \tag{3.31}$$

A simulation proved that

$$U_{\text{out}} \approx \begin{cases} 2.4132\ \text{mV} & \Leftrightarrow \text{spin valve is at high resistance.} \\ \\ 2.1557\ \text{mV} & \Leftrightarrow \text{spin valve is at low resistance.} \end{cases} \tag{3.32}$$

[7]The value of R_7 can be chosen arbitrarily. It forms a voltage divider with the spin valve. For simplicity in the case study it was chosen to be equal to R_{AP}. In this situation half of the sensing voltage drops over the spin valve if the spin valve is set to R_{AP}.

The deviation between the simulated and the expected voltages is approximately 3.5%. Yet, the origin of the deviation is unclear, but it is suspected that it is due to the sensing voltage.

Summary

The circuit matches some of the quality criteria for compact models (cf. Sec. 2.5):

- The key property of a compact model is its simplicity at a desired degree of accuracy. The circuit consists of only six resistors, two voltage sources, one operational amplifier and one transistor; therefore it is a simple model for the hysteresis of a spin valve.
- The hysteresis of a spin valve's resistance is approximated through a rectangular-shaped voltage.
- The circuit is predictive at a quite high degree of accuracy.
- Both case studies together substantiate the flexibility of the circuit. Parameters can be set so as to match the experimental situation.
- The circuit can provide new insights into the function, performance characteristics, and limits of systems based on spin valves (cf. Sec. 3.2).

In contrast to real spin valve, the circuit is an active device because an operational amplifier and a transistor are used. At an input voltage of 0 V (or equivalently 0 A) the circuit will behave properly, however the supply voltages of the operational amplifier must not be switched off during operation. On the other hand these supply voltages have to be excluded when the power consumption of the circuit is compared with that of a real spin valve.

The spin valve is modeled as a device with three terminals similar to a transistor. The voltage to program the resistance can be chosen independently from the sensing voltage. Such a distinction is valid for real *field-driven* spin valves. Here the spin valve is programmed with an Oersted field due to a programming current. The wire that carries the programming current is electrically isolated from the spin valve. The voltage drop over the spin valve is entirely determined by the sensing signal (current or voltage) and the resistance of the spin valve. Attention must be paid to the choice of programming and sensing voltage. A realistic sensing voltage must be chosen such that the voltage drop over a spin valve does not alter the resistance. The sensing voltage depends on the thresholds of the individual spin valve to be mimicked. At present it is possible to use a sensing voltage far beyond the valid range without altering the resistance of the spin-valve circuit.

- The resistance of a spin valve after Albert *et al.* (case study 1) switches at a current of +1.7 mA from low to high. The highest voltage that corresponds to this current is $U = R_{AP} \cdot I = 1.59\ \Omega \cdot 1.7\ \text{mA} = 2.7030\ \text{mV}$. At sensing voltages greater or equal to 2.7030 mV the real spin valve would be programmed to high resistance. A voltage drop of 2.5 mV corresponds to a current of approximately 1.6234 mA. If the resistor R_7 is dimensioned to be equal to R_{AP}, half of the sensing voltage drops over the spin valve; therefore a reasonable sensing voltage is 5 mV.
- For a spin valve after Kawahara *et al.* (case study 2, resistances 5 kΩ in the low resistance state and 7 kΩ in the high resistance state) the maximal positive voltage

drop without switching the resistance is $U = R_{AP} \cdot I = 7\ \mathrm{k\Omega} \cdot 200\ \mu\mathrm{A} = 1.4000\ \mathrm{V}$. A sensing voltage of 0.7 V is appropriate, since the resistance of the real spin valve is not altered then.

In a real *current-driven* spin valve the separation between programming current and sensing current does not apply. There is just one current flowing across the spin valve. For this reason the programming current in the work of Kawahara *et al.* is a pulse with three different levels, one for programming low resistance, one for programming high resistance, and one for sensing. (cf. the inset of Fig. 3.6 and Fig. 3.7). For sensing the programming signal may be set to 0 A; then the resistance can be sensed correctly at the SENSE terminal. That implies that the resistance of a current-driven spin valve can never be sensed while it is programmed. Again the sensing voltage must not alter the state of the spin valve. The results from the simulations (Fig. 3.5 - 3.8) apply to current-driven spin valves only if the programming signal is chosen appropriately.

Using an equivalent circuit to mimic a spin valve is pretty obvious, because the spin valve is intended to be used for circuit design. The circuit however does not reflect all properties of a spin valve that are relevant for circuit design yet. For instance the circuit cannot be used for simulations if a spin valve is operated as an oscillator.

Attention must also be paid to the switching points. For given switching points $U_{\mathrm{in,off}}$ and $U_{\mathrm{in,on}}$ the supply voltages U_+ and U_- as well as the resistors R_1 and R_2 have to be dimensioned. The range of the allowed input voltage is determined by the supply voltages. Valid input voltages lie in the interval defined by the supply voltages. For a wide range of the input voltage, a comparatively large positive supply voltage and a comparatively small negative supply voltage are inevitable. As can be seen from Eq. 3.2, the switching point closest to 0 V determines also the supply voltage that controls the other switching point because of the ratio $\frac{U_{\mathrm{in,off}}}{U_+} = \frac{U_{\mathrm{in,on}}}{U_-}$. Assuming that the switching point $U_{\mathrm{in,off}}$ is close to 0 V; in this case the ratio $\frac{U_{\mathrm{in,off}}}{U_+}$ is small with large values of U_+. This holds similarly for $U_{\mathrm{in,on}}$ and U_-. A larger switching point allows choosing a larger supply voltage. An example (using an inverting Schmitt trigger) underlines that:

- The switching point from "high" output voltage to "low" output voltage is $U_{\mathrm{in,off}} = 1.7$ V (spin valve after Albert *et al.*).
- The positive supply voltage shall be $U_+ = 13$ V.
- The switching point from "low" output voltage to "high" output voltage is $U_{\mathrm{in,on}} = -4.3$ V.
- The resulting negative supply voltage then would be $U_- = -32.8828$ V (using Eq. 3.2). This value is beyond the range of many operational amplifiers (the LM8261 allows maximum supply voltages of ± 30 V [203]).

Reducing the positive supply voltage to $U_+ = 10$ V yields a different negative supply voltage U_- with the given switching points. Now $U_- = -25.2939$ V (again Eq. 3.2 was used). Valid input voltages are now within the interval between -25.2939 V and 10 V. If a larger range of the input voltage is desired, either the mapping the mapping 1 mA $\widehat{=}$ 1 V has got to be dismissed or a different operational amplifier with different supply voltages is necessary (which is not always possible). There are no objections against a limitation of the allowed input voltage, as long as the hysteresis loop is mimicked completely. If the switching points are symmetrical around 0 V, like for spin valve after Kawahara *et al.*, the supply voltages are also symmetrical and can be chosen with the specified range for the operational amplifier.

3.2 Prototypical implementation of a NAND and a NOR gate using the compact model for the idealized hysteresis

As explained in Sec. 2.3 spin valves have been proposed for building logic gates for some time. Two different approaches are dominant. In the first approach a single spin valve is used. Each Boolean input is represented through the amplitude of an electric current on a wire on top of the spin valve. Several works make use of this approach [107–111]. All relevant Boolean functions, like AND, OR, NAND and NOR can be implemented. The second approach to implement logic gates was proposed by Richter *et al.*; here four spin valves form one logic gate. The spin valves are divided into an input and a reference branch [114–116]. The input branch is a series of two spin valves, whose resistance is determined or programmed by the two inputs of the gate. The reference branch also consists of two spin valves in series. Their resistance is determined (or programmed) before the gate can be used; the state of the reference branch remains unchanged during operation.

Based on the latter concept and the equivalent circuit for spin valves whose resistance shows a rectangular-shaped hysteresis, the implementation of a NAND gate and a NOR gate is described in the following. The implementation of the gates is demonstrated with the two case studies from above: first, the resistances of each spin valve are chosen similar to those measured by Albert *et al.* [147]; low resistance is equivalent to 1.54 Ω and high resistance corresponds to 1.59 Ω. The subsequent example is based on the work by Kawahara *et al.* [96]; the low resistance is assumed to be 5 kΩ and the high resistance is 7 kΩ.

The circuit mimicking a single spin valve is shown in Fig. 3.1, while Fig. 3.9 shows the respective graphic symbol. The input signal (which determines the resistance of a spin valve) can be either an applied magnetic field or an electric current. In the circuit both, the field and the current are represented by a voltage, which is applied between the terminal PROG and ground. The only difference between field-driven and current-driven spin valves is the shape of the programming signal. For a field-driven spin valve the programming signal is a

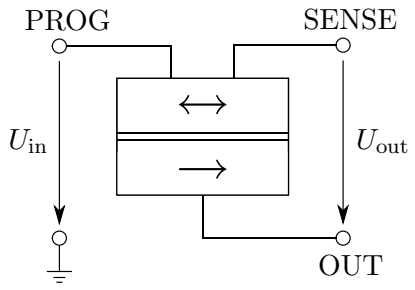


Figure 3.9: Circuit symbol for a single spin valve. The input signal, which determines the resistance of the spin valve, is the voltage between the terminal PROG and ground. The resistance of the spin valve is expressed through the voltage between SENSE and OUT.

rectangular-shaped pulse, which switches between two values. The programming signal for current-driven spin valve is a pulse with three different levels, one for programming low resistance, one for programming high resistance, and one for sensing. (cf. the inset of Fig. 3.6 and Fig. 3.7). Each spin valve is programmed with a pulse before the gate's output can be determined. Kawahara *et al.* program the spin valves in their memory module with a pulse of 100 ns. To measure the resistance, a voltage divider is used. The corresponding voltage drops between the terminals SENSE and OUT. The distinction between the programming voltage and the sensing voltage corresponds to the distinction between reading and writing the state of the spin valve. This partition is emphasized by the structure of the circuit for a single spin valve. As mentioned above, an arbitrary sensing voltage could undesirably alter the resistance of the spin valve. Such a voltage drop over the spin valve due to the sensing voltage lies outside the range for sensing the resistance of the spin valve (which is defined by the thresholds of the hysteresis). In the following examples the voltage drop over the spin valve for sensing is always valid (i.e. the voltage drop over the spin valve would not alter its state in reality).

The gate is supposed to have two Boolean inputs A and B. The circuit for mimicking a logic gate is shown in Fig. 3.10. The two upper spin valves process the two Boolean inputs. The logical value 1 is represented through a voltage of +5 V and the logical value 0 through a voltage of −5 V. This assignment can changed to match with real spin valves. The results of the simulations however are valid regardless of the validity of the input signals as long as the resistances and the sensing voltages are set correctly. The difference in the resistances between the input branch on the left-hand side and the reference branch on the right-hand side is the gate's output U_{out}.

The following results can directly be applied to field-driven spin valves. The only difference to mimicking current-driven spin valves is the shape of the inputs A and B and a small delay before the output signal can be measured[8]. The inputs A and B are represented through rectangular pulse voltages U_A and U_B. Each voltage source switches from −5 V to +5 V. Input A has a pulse width of 1 ms, input B of 2 ms. Rise and fall time of the pulses for both inputs are 10 µs. U_1 is a DC voltage source of +5 mV and $R_1 = 1.59\ \Omega$. Together with SV_1 and SV_2, R_1 forms a voltage divider. The voltage over the input branch is U_x. The reference branch on the right-hand side of Fig. 3.10 consists of the spin valves SV_3 and SV_4. U_2 is also a DC voltage of +5 mV. Similar to R_1, $R_2 = 1.59\ \Omega$ for the first case study. In the second example R_1 and R_2 are set to 7 kΩ; U_1 and U_2 are set to 0.7 V. The spin valve SV_3 is programmed to high resistance, whereas SV_4 is programmed to low resistance. To achieve this the voltage U_{ref1} is set to −5 V and U_{ref2} to +5 V. R_2, SV_3, and SV_4 form the other voltage divider. The voltage over the reference branch is U_y. Based on the state of the spin valves SV_3 and SV_4 either the NAND or the NOR function can be programmed. In the latter

[8]Instead of a pulse with two levels, for current-driven switching a pulse with three levels is necessary, one for programming low resistance, one for programming high resistance, and one level for sensing. The respective gate is programmed with a short pulse at the beginning; immediately after programming, the input is set to 0 A (in the circuit 0 V). Then the output of the spin valve can be determined by the sensing voltage.

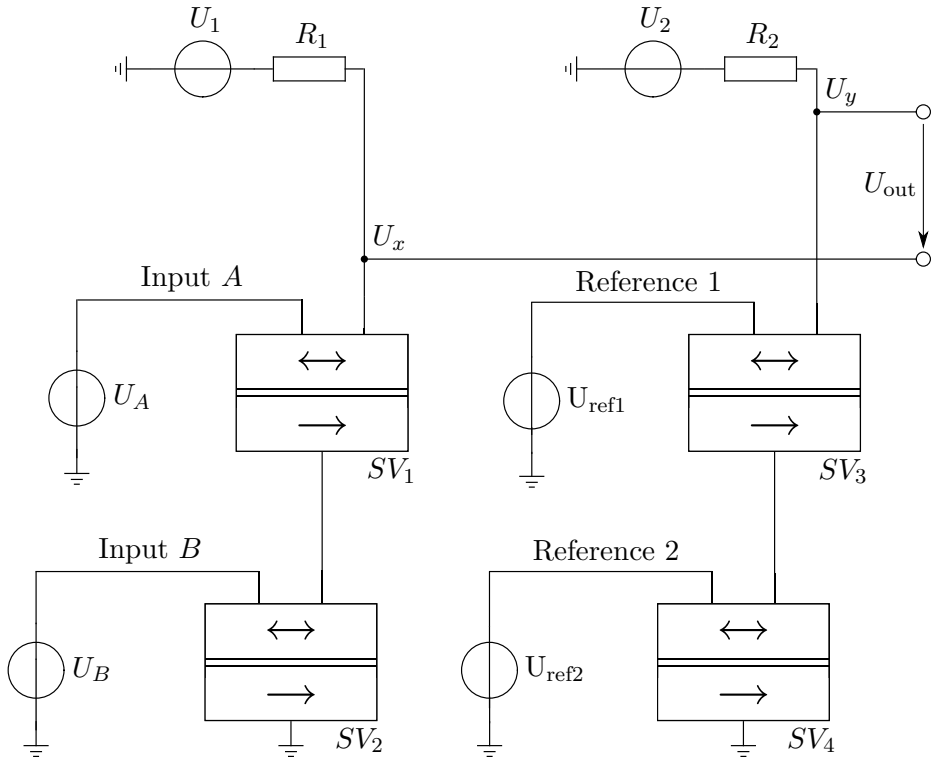


Figure 3.10: Circuit for a logic gate according to the concept of Richter *et al.* The inputs A and B are represented through the voltages U_A and U_B. R_1, SV_1, and SV_2 form a voltage divider; the voltage over the input branch is U_x. The reference branch consists of SV_3 and SV_4, which are programmed via U_{ref1} and U_{ref2}. R_2, SV_3, and SV_4 also form a voltage divider. The voltage over the reference branch is U_y. The output of the gate is $U_{\text{out}} = U_y - U_x$.

case both spin valves are programmed to have the low resistance. The output of the gate is

$$U_{\text{out}} = U_y - U_x. \tag{3.33}$$

The results from simulations for the first case study are shown in Fig. 3.11 and Fig. 3.12. A voltage of +5 V at the input of a spin valve will program the resistance to "high"; a voltage of −5 V will lead to "low" resistance. The time scale is determined by the used operational amplifier. For the simulations the LM8261 from National Semiconductor was used [203]. This amplifier possesses a gain bandwidth product of 21 MHz. The gain bandwidth product determines the maximum gain that can be extracted from the operational amplifier for a given frequency or bandwidth. In order to study state-of-the-art spin valves, the circuit should allow to simulated clock frequencies in the order of some GHz. At present, the circuit allows clock frequencies in the order of kHz. It is therefore essential to enhance the circuit in this respect.

Summary

The transient diagrams (Fig. 3.11 and Fig. 3.12) indicate that both gates implement the respective logical function properly when a spin valve (with similar resistances to the work of Albert *et al.*) is used. The netlist can be found in appendix A.3. The maximal clock rates depend on the gain bandwidth product of the amplifier. The exact values for the output voltages are listed in Tab. 3.1.

Threshold voltages must be defined in order to distinguish whether if the output voltage of a gate corresponds to logical value 1 or 0. As Tab. 3.1 shows the smallest voltage to represent a logical 1 is 0 V. The largest voltage representing a logical 0 is $-1.748 \cdot 10^{-5}$ V. Based on these results, the following thresholds were chosen:

- If $U_{\text{out}} > -0.2 \cdot 10^{-5}$ V, the output of a gate is interpreted as the logical value 1.
- If $U_{\text{out}} < -1.6 \cdot 10^{-5}$ V, the output of a gate is interpreted as the logical value 0.
- The output voltage must not lie within the range from $-1.6 \cdot 10^{-5}$ V to $-0.2 \cdot 10^{-5}$ V. Any output voltage in this interval is a forbidden value.

logical inputs (A, B)	logical output		corresponding output in V	
	NAND	NOR	NAND	NOR
$(0, 0)$	1	1	$1.795 \cdot 10^{-5}$	0
$(1, 0)$	1	0	$9.1 \cdot 10^{-8}$	$-1.786 \cdot 10^{-5}$
$(0, 1)$	1	0	0	$-1.795 \cdot 10^{-5}$
$(1, 1)$	0	0	$-1.748 \cdot 10^{-5}$	$-3.543 \cdot 10^{-5}$

Table 3.1: Output voltages of both gates for every configuration of the inputs when spin valves similar to the work of Albert *et al.* are used. The output voltages are obtained for sensing voltages $U_1 = U_2 = 5$ mV and resistors $R_1 = R_2 = 1.59\ \Omega$ (cf. Fig. 3.10). In this case the voltage drop over each branch is of the order of 3.5 mV. Assuming that both spin valves are programmed to low resistance ($= 1.54\ \Omega$), this yields the maximum current of approximately 1.15 mA, which is well below the threshold of 1.7 mA.

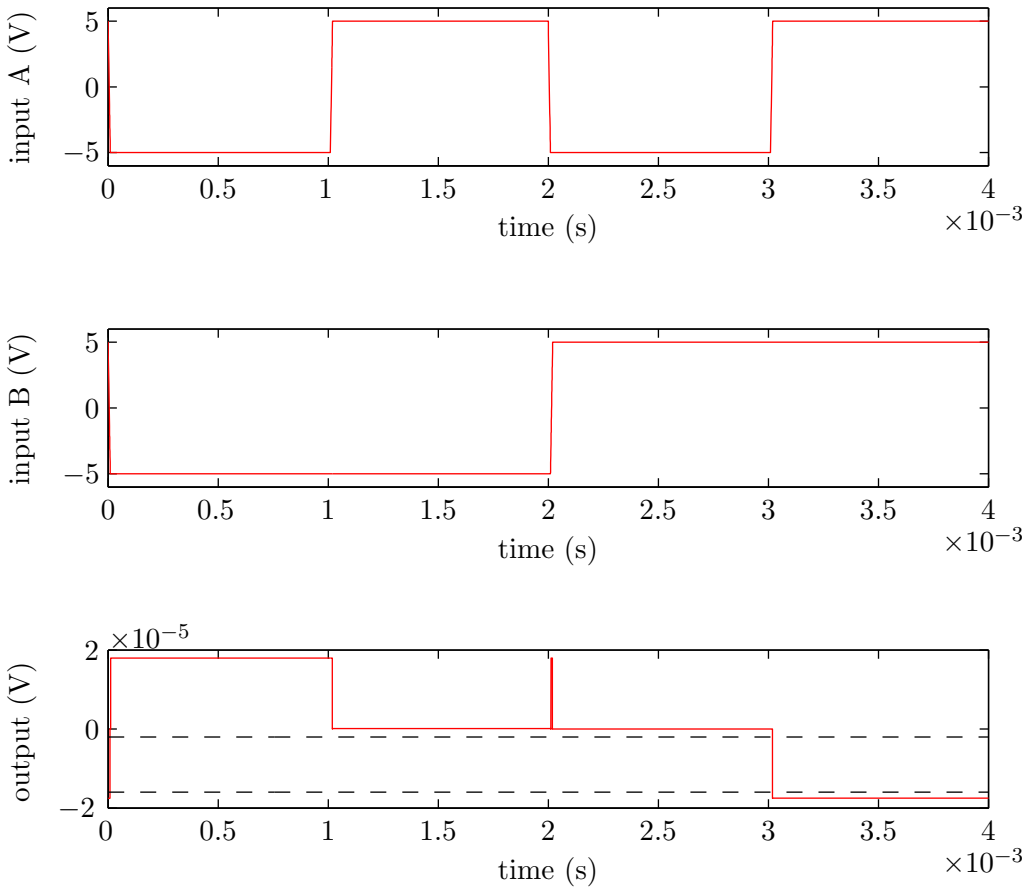


Figure 3.11: Transient diagram of the NAND gate after Richter *et al.* [114] employing the equivalent circuit for a rectangular-shaped hysteresis curve for a spin valve similar to the work of Albert *et al.* [147]. The inputs are A and B; both inputs are rectangular-shaped pulses with a pulse width of 1 ms for input A, and a pulse width of 2 ms for B. Rise and fall time of the pulses for both inputs are 10 µs. The logical value 0 is represented through a voltage of -5 V; the logical value 1 through a voltage of $+5$ V. The output voltage is depicted for every possible configuration of the inputs. The sensing voltages for the input and reference branch are $+5$ mV; $R_1 = R_2 = 1.59\ \Omega$ (cf. Fig. 3.10). The peak at 2 ms is due to the timing of the inputs and their edges. The spin valve SV_3 is programmed to low resistance, whereas SV_4 is programmed to have high resistance. In order to distinguish between both logical values, thresholds were defined (indicated by the dashed horizontal lines). If the gate's output voltage is greater than the upper threshold, it is interpreted as a logical 1; if the output voltage is less than the lower threshold, it corresponds to a logical 0. The intermediate zone between the thresholds is forbidden. The clock frequencies used in the simulations do not match today's demands of clock rates of some GHz, albeit the resulting voltage drops are reasonable.

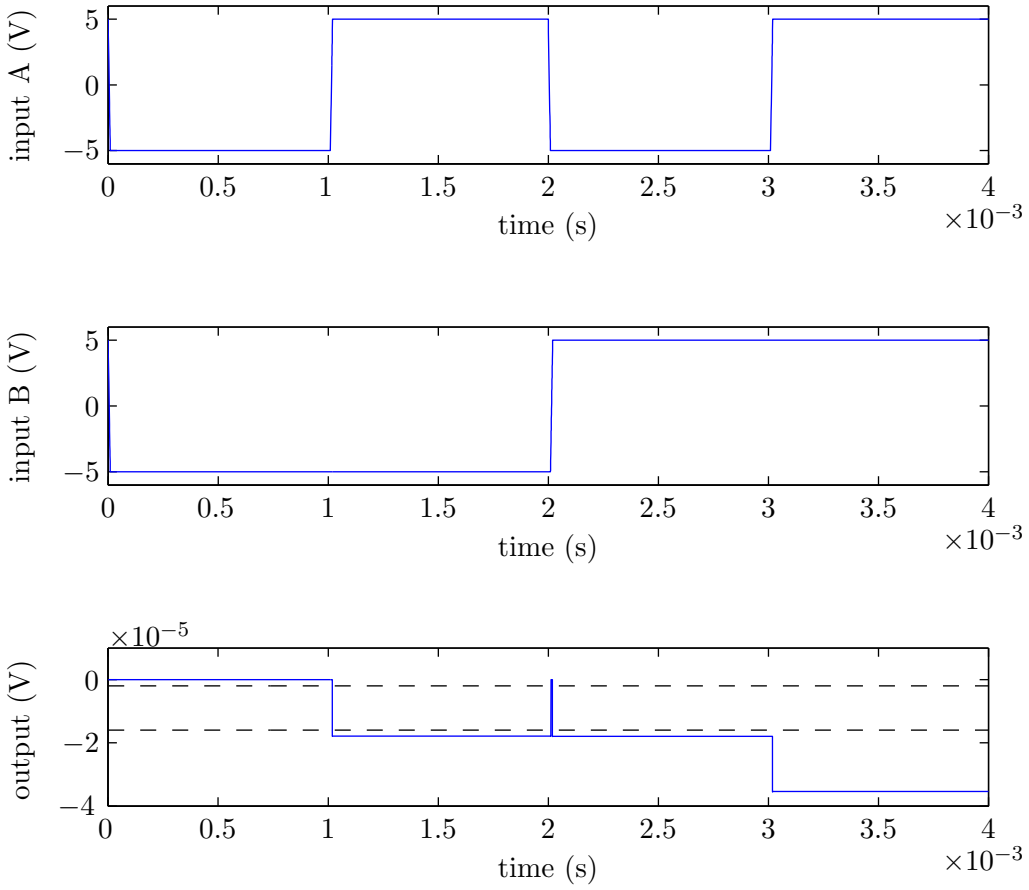


Figure 3.12: Transient diagram of the NOR gate after Richter *et al.* [114] employing the equivalent circuit for a rectangular-shaped hysteresis curve for a spin valve similar to the work of Albert *et al.* [147]. The inputs are A and B; both inputs are rectangular-shaped pulses with a pulse width of 1 ms for input A, and a pulse width of 2 ms for B. Rise and fall time of the pulses for both inputs are 10 µs. The logical value 0 is represented through a voltage of −5 V; the logical value 1 through a voltage of +5 V. The output voltage is depicted for every possible configuration of the inputs. The sensing voltages for the input and reference branch are +5 mV; $R_1 = R_2 = 1.59\ \Omega$ (cf. Fig. 3.10). The peak at 2 ms is due to the timing of the inputs and their edges. Both reference cells are programmed to have low resistance. In order to distinguish between both logical values, thresholds were defined (indicated by the dashed horizontal lines). If the gate's output voltage is greater than the upper threshold, it is interpreted as a logical 1; if the output voltage is less than the lower threshold, it corresponds to a logical 0. The intermediate zone between the thresholds is forbidden. The clock frequencies used in the simulations do not match today's demands of clock rates of some GHz, albeit the resulting voltage drops are reasonable.

If a logic gate with spin valves similar to the work of Kawahara *et al.* [96] is mimicked by the equivalent circuit, different output voltages are obtained. Table 3.2 shows the exact values of the output voltages of the gate. For these voltages sensing voltages of +0.7 V (U_1, U_2) are assumed. Furthermore, the resistors R_1 and R_2 are chosen to be equal to 7 kΩ. Figures 3.13 and 3.14 show the transient diagrams for the gates. Threshold voltages for distinguishing the output voltage between logical values 1 and 0 are defined as follows. Table 3.2 shows that the smallest voltage to represent a logical 1 is 0 V. The largest voltage representing a logical 0 is −0.02434 V. Based on these results, the following thresholds were chosen:

- If $U_{\text{out}} > -7.5$ mV, the output of a gate is interpreted as the logical value 1.
- If $U_{\text{out}} < -20$ mV, the output of a gate is interpreted as the logical value 0.
- The output voltage must not lie within the range between −20 mV and −7.5 mV. Any output voltage in this interval is a forbidden value.

logical inputs (A, B)	logical output		corresponding output in V	
	NAND	NOR	NAND	NOR
$(0, 0)$	1	1	0.03023	0.0004626
$(1, 0)$	1	0	0.000108	−0.03012
$(0, 1)$	1	0	0	−0.03023
$(1, 1)$	0	0	−0.02434	−0.05457

Table 3.2: Output voltages of both gates for every configuration of the inputs when spin valves similar to the work of Kawahara *et al.* are used. The output voltages are obtained for sensing voltages $U_1 = U_2 = 0.7$ V and resistors $R_1 = R_2 = 7$ kΩ (cf. Fig. 3.10). In this case the voltage drop over each branch is of the order of 0.5 V. Assuming that both spin valves are programmed to low resistance (= 5 kΩ), this yields the maximum current of approximately 50 µA, which is well below the threshold of 200 µA.

Although the gates work properly they are not able yet to drive other gates because of the comparatively small output voltages. The results suggest that the higher the resistances of a spin valve are, the higher the output voltage of the gate will be. A closer look at the two case studies from above reveals:

- The highest resistance in the first case study (spin valves after Albert *et al.*) is assumed to be 1.59 Ω.
- The highest resistance in the second case study (Kawahara *et al.*) is in return assumed to be 7 kΩ.
- The ratio between both resistances is approximately $4,400$.
- The highest output voltages in both case studies can be compared by normalizing the output voltage for a logic gate after Kawahara *et al.* with respect to the first case study

(because of the different sensing voltages). The normalized highest output voltage in the second case study is

$$\frac{U_{\text{sense, Albert}}}{U_{\text{sense, Kawahara}}} \cdot 0.03023\ \text{V} = 7.143 \cdot 10^{-3} \cdot 0.03023\ \text{V} = 2.1593 \cdot 10^{-4}\ \text{V};$$

compared to the highest output voltage in the first case study ($+1.795 \cdot 10^{-5}$ V), this is only the twelve-fold magnification.

As a result it is found that the sensing voltages have a strong influence on the gate's output voltage. Increasing the sensing voltages is possible only if the resulting current through one of the spin valves in the circuit would not alter the resistance of the corresponding spin valve (cf. Fig. 3.4); otherwise the results from the circuit allow no predictions of the characteristics of a similar gate fabricated with the respective spin valves. Current-driven spin valves can be simulated just by adjusting the shape of the programming signal.

Even with appropriate sensing voltages one problem of Richter's concept however remains. This problem is due to the structure of the gate: the output voltage of the gate is the difference between the voltage drops over the input and reference branch. No matter what the sensing voltages or the resistances are like, there will always be logical outputs that are represented by a voltage equal or close to zero. In such a situation the gate still might not be able to drive other gates, for example in a flip-flop. This holds also for logic gates after Ney *et al.* [107]. Additional circuitry is thus inevitable. A proper solution to increase the output voltage of the logic gate would be to use a comparator (e.g. implemented with an operational amplifier). The comparator would convert the output voltage of the gate to a desired value. A more flexible way to implement a logic gate would be a look-up table. It consists of an n-Bit memory and an $n : 1$ multiplexer [204]. The Boolean function is not implemented through the comparison of two voltages like in Richter's gate, but through the state of an addressable memory cell. In the context of field-programmable gate arrays look-up tables have established themselves because of their flexibility compared to hard-wired logic gates. In his Diploma thesis Tobias Kipp (from the Research group Computer Engineerung, University of Hamburg) has designed look-up tables based on the equivalent circuit for spin valves that is described in Sec. 3.1 [205]. The maximum clock frequency of the logic gate is determined by the components of the circuit that mimics the spin valve (see comment after Eq. 3.33).

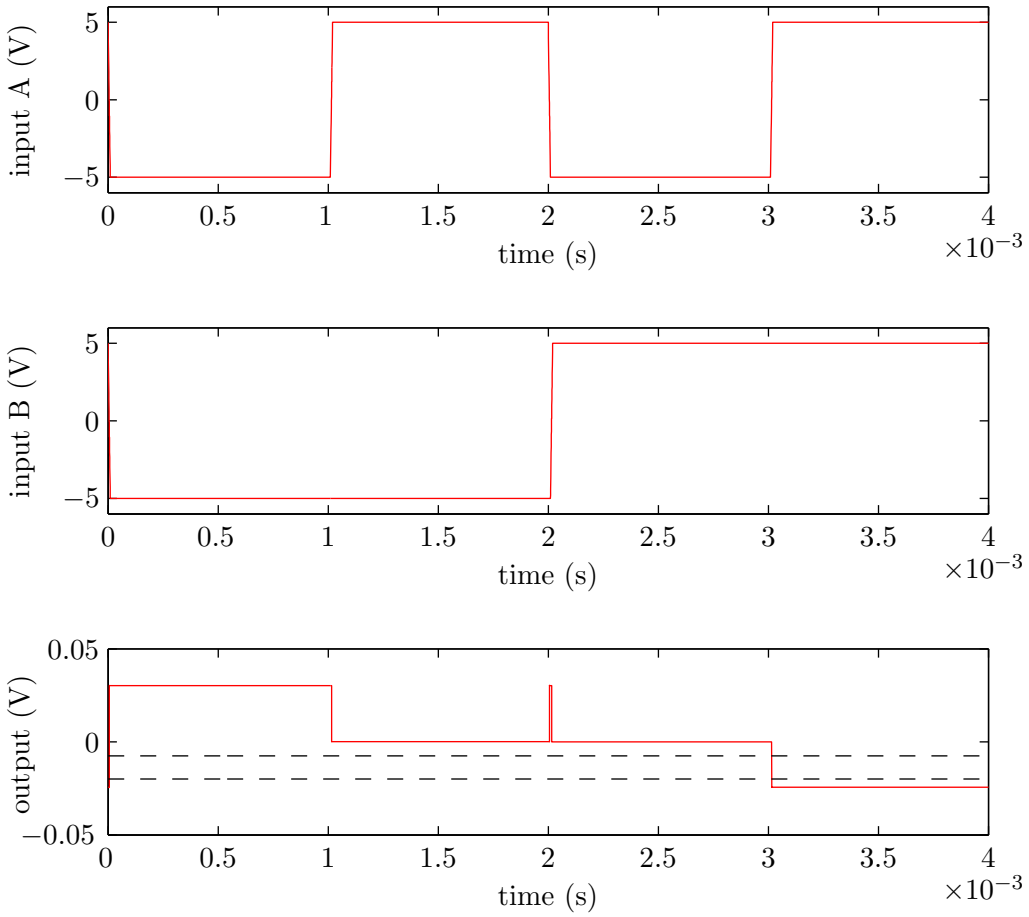


Figure 3.13: Transient diagram of the NAND gate after Richter *et al.* [114] employing the equivalent circuit for a rectangular-shaped hysteresis curve for a spin valve similar to the work of Kawahara *et al.* [96]. The inputs are A and B; both inputs are rectangular-shaped pulses with a pulse width of 1 ms for input A, and a pulse width of 2 ms for B. Rise and fall time of the pulses for both inputs are 10 µs. The logical value 0 is represented through a voltage of -5 V; the logical value 1 through a voltage of $+5$ V. The output voltage is depicted for every possible configuration of the inputs. The sensing voltages for the input and reference branch are $+0.7$ V and $R_1 = R_2 = 7$ kΩ (cf. Fig. 3.10). The peak at 2 ms is due to the timing of the inputs and their edges. The spin valve SV_3 is programmed to low resistance, whereas SV_4 is programmed to have high resistance. In order to distinguish between both logical values, thresholds were defined (indicated by the dashed horizontal lines). If the gate's output voltage is greater than the upper threshold, it is interpreted as a logical 1; if the output voltage is less than the lower threshold, it corresponds to a logical 0. The intermediate zone between the thresholds is forbidden.

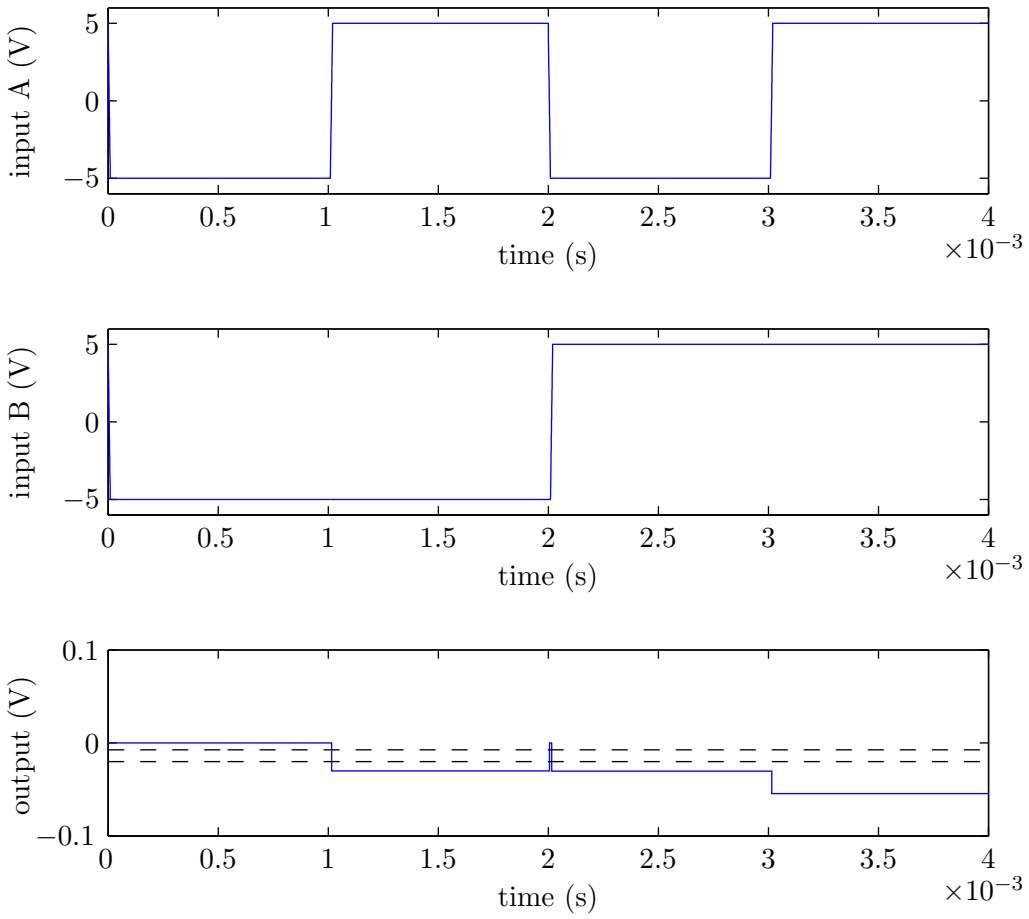


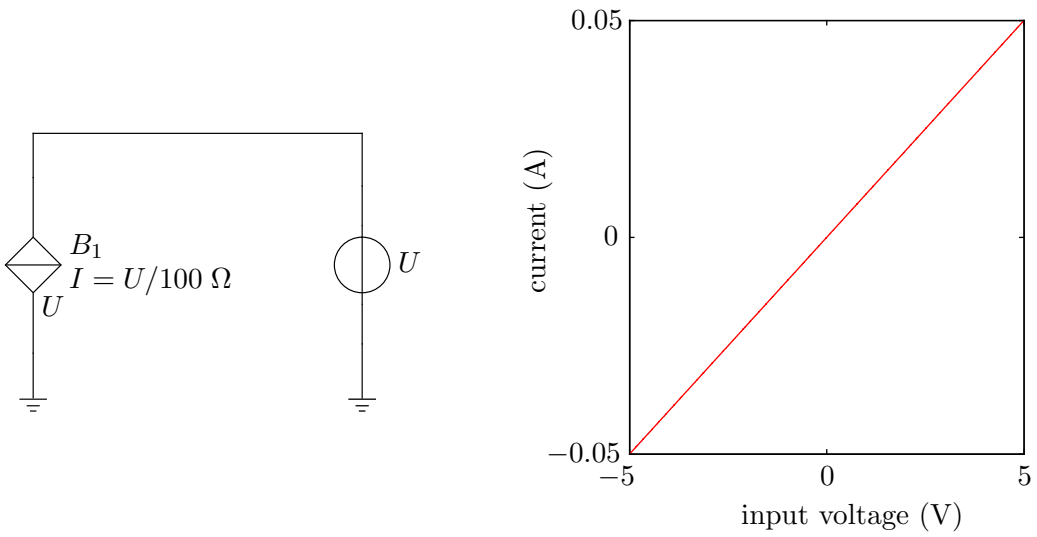
Figure 3.14: Transient diagram of the NOR gate after Richter *et al.* [114] employing the equivalent circuit for a rectangular-shaped hysteresis curve for spin valve similar to the work of Kawahara *et al.* [96]. The inputs are A and B; both inputs are rectangular-shaped pulses with a pulse width of 1 ms for input A, and a pulse width of 2 ms for B. Rise and fall time of the pulses for both inputs are 10 µs. The logical value 0 is represented through a voltage of -5 V; the logical value 1 through a voltage of $+5$ V. The output voltage is depicted for every possible configuration of the inputs. The sensing voltages for the input and reference branch are $+0.7$ V and $R_1 = R_2 = 7$ kΩ (cf. Fig. 3.10). The peak at 2 ms is due to the timing of the inputs and their edges. Both reference cells are programmed to have low resistance. In order to distinguish between both logical values, thresholds were defined (indicated by the dashed horizontal lines). If the gate's output voltage is greater than the upper threshold, it is interpreted as a logical 1; if the output voltage is less than the lower threshold, it corresponds to a logical 0. The intermediate zone between the thresholds is forbidden.

3.3 Compact model for a spin valve with a realistic hysteresis

The text in the following section is based partially on the manuscript "A Compact Model for Spin Valves in Computing Devices" (Ref. [206]) that is submitted for publication to IEEE Transactions on Circuits and Systems I: Regular Papers. The manuscript was written in cooperation with Benjamin Krüger (I. Institute for Theoretical Physics, University of Hamburg, Germany), Massoud Najafi, Tobias Kipp, Professor Dr.-Ing. Dietmar P. F. Möller (Research group Computer Engineering, University of Hamburg), and Dr. Scott Roy (Device Modelling Group, University of Glasgow, United Kingdom). The idea for the following circuit was first developed during my work in the interdisciplinary research training group (Graduiertenkolleg) 1286 "Functional Metal-Semiconductor Hybrid Systems" (speaker Professor Dr. Ulrich Merkt) and then later refined during a research stay with the Device Modelling Group in July and August 2009. Prior to the publication of the manuscript, this section provides first intermediate results.

The equivalent circuit mimicking a rectangular-shaped hysteresis of a spin valve's electrical resistance is an approximation of the actual hysteresis (cf. the measured hysteresis curves for both case studies in Sec. 3.1). This circuit was designed to be as simple as possible. Such an approximation already allows estimating the ability of a spin valve to perform storage and logic operations. It is reasonable for a feasibility study to approximate the behavior, since an approximation reduces the complexity of both the circuit and the simulation. For an in-depth analysis however, an approximate hysteresis might not be adequate. In the following the design of a different equivalent circuit for spin valves is depicted with slightly more components, but with a tunable accuracy of the hysteresis. Again, at the input stage of the circuit the current that is responsible for switching the resistance of a spin valve is mapped onto a voltage. The electrical resistance of the spin valve is expressed through the corresponding voltage drop. Figure 3.15 depicts an electrical circuit equivalent to an Ohmic resistor with a resistance of 100 Ω. Similar to the following spin-valve circuit, the resistor is modeled as a current source, where the current depends on the applied voltage. The netlist for the Ohmic resistor is shown in the appendix A.4. For the following spin-valve circuit it is essential to use non-linear controlled sources. These are provided in SPICE as elements with the identifier B. The non-linear controlled source may either be current or voltage sources. Apart from the switching points (that is, the input signals at which the resistance switches between "low" and "high") a hysteresis curve consists of an upper branch and a lower branch. The idea of the new circuit is to separate the switching between "high" and "low" resistance from the representation of lower and upper branch of the hysteresis. The circuit consists of four components:

- a current-to-voltage converter (in terms of a linear current-controlled voltage source),
- a Schmitt trigger to switch between "high" and "low" resistance,
- a non-linear voltage-controlled voltage source to represent the lower branch as well as
- a non-linear voltage-controlled voltage source to represent the upper branch.



(a) (b)

Figure 3.15: Equivalent circuit for an Ohmic resistor with a resistance of 100 Ω. (a): Circuit diagram. B_1 is a non-linear voltage-controlled current source, the voltage source U generates the input voltage. (b): Plot of the current depending on the input voltage (the input voltage is swept from −5 V to +5 V).

The two latter voltage sources are controlled with the input voltage of the circuit. The Schmitt trigger generates a control signal which can attain two values. It drives a pair of field-effect transistors, which are complementary to each other. Each transistor either suppresses the signal for the corresponding branch or not. At any instant of time the voltage from one branch is suppressed while the other drops at the output stage depending on the input voltage. There are other recent publications on equivalent circuits mimicking spin valves that follow the same concept. The circuit presented here is more flexible than the circuit by Lee *et al.* [184], who assumed the lower branch of the hysteresis to be constant. Apart from the implementation of the operational amplifier the circuit by Mukherjee and Kurinec [5] consists of more components than the circuit that is described subsequently. The circuit mimics a spin valve after Albert *et al.* [147]. The authors demonstrate current-induced switching of a spin valve's resistance that may be the dominant mechanism for switching in the future. Furthermore, the difference between both resistance states is approximately only 0.06 Ω. In the experiment the current is swept in the direction from the negative maximum to the positive maximum and again in opposite direction. The former case is referred to as the upsweep and the latter sweep is referred to as the downsweep. For each sweep this results in a step function. The hysteresis curve is characterized as follows (cf. also page 37):

1. There exist two resistances R_L and R_H with $R_L < R_H$
2. There is one switching point S^+ to switch from R_L to R_H.
3. There is one switching point S^- to switch from R_H to R_L

4. For the switching points $S^+ > S^-$ holds.

The resistances R_L and R_H correspond to the parallel and antiparallel alignment of the magnetization in the free layer of the spin valve relative to that of its fixed layer. For each sweep Albert *et al.* have measured the differential resistance. The dimensioning of the circuit requires fit functions for the resistance. The fit functions are based on data points, which are restored from an image of Fig. 2(a) in the work of Albert *et al.* (Ref. [147]) at a resolution of 72 dpi due to the lack of more accurate data. Both fit functions are listed in appendix A.5. Figure 3.16 shows the restored data points.

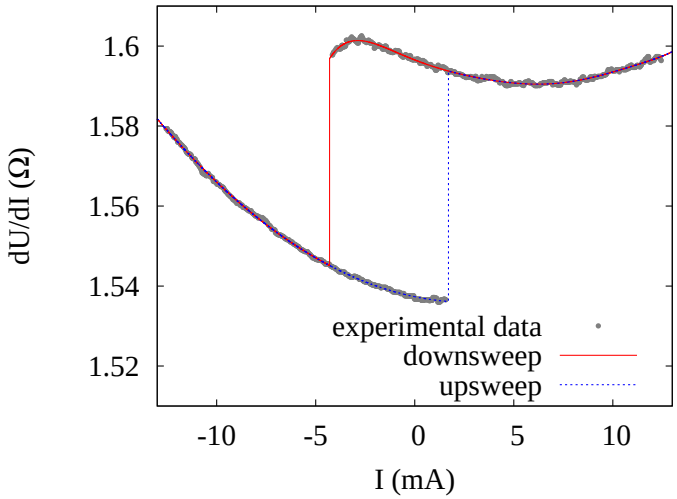


Figure 3.16: Hysteresis curve extracted from [147]. The differential resistance dU/dI in Ω is plotted against the current I in mA that flows through the spin valve. The reconstructed data points are illustrated by the gray • symbols. On the basis of the data points the differential resistance is depicted during the upsweep (blue dashed line) and during the downsweep (solid red line). The underlying fit functions for the low and high resistance state are listed in appendix A.5. At an input current of $I_C^+ = 1.7$ mA the resistance of the spin valve switches from low resistance to high resistance during the upsweep. The resistance switches from high resistance to low resistance at an input current of $I_C^- = -4.3$ mA during the downsweep.

If the differential resistance in the low and high resistance states is integrated with respect to the applied current, the integration yields two functions for the voltage drop over the spin valve, one for the low resistance state and the other for the higher resistance state; both are shown in Fig. 3.17. A Schmitt trigger is used to generate a control signal that allows for a distinction between both branches, similar to the previous work (Ref. [196]). If the output of the Schmitt trigger corresponds to the low resistance state, the signal for the upper branch is suppressed and vice versa. With this mechanism one can recover the hysteresis of the voltage (cf. Fig. 3.17 and Fig. 3.25). Similar to the circuit that mimics an idealized rectangular-shaped hysteresis, the current, which is responsible for switching is mapped onto an input voltage in the circuit. From the experimental data in [147] one can find: The spin valve switches from low resistance R_L to high resistance R_H at an input current $I_C^+ = 1.7$ mA

which corresponds in the circuit to an input voltage $U_C^+ = 1.7$ V. The resistance of the spin valve switches from R_H to R_L at an input current $I_C^- = -4.3$ mA. This current corresponds to an input voltage $U_C^- = -4.3$ V in the circuit.

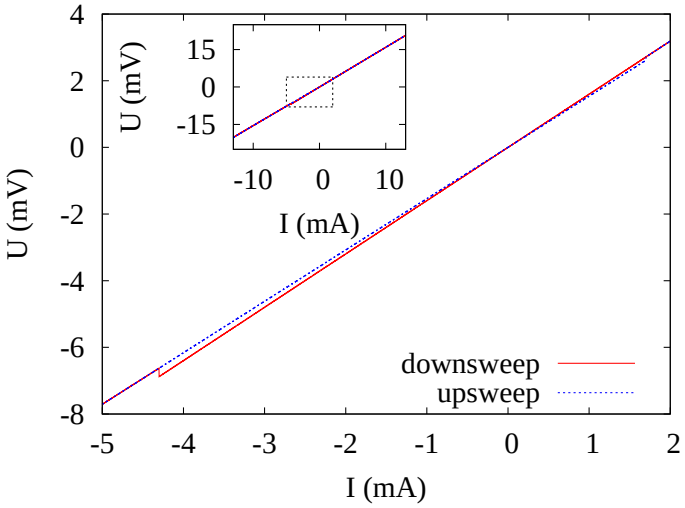


Figure 3.17: Voltage drop over the spin valve versus applied current. The voltage is obtained by integrating the differential resistance dU/dI with respect to the current I. On the basis of experimental reference data (Ref. [147]) fit functions for the differential resistance in the low and high resistance state were determined and then integrated. At an input current of $I_C^+ = 1.7$ mA the resistance of the spin valve switches from low resistance to high resistance during the upsweep. The resistance switches from high resistance to low resistance at an input current of $I_C^- = -4.3$ mA during the downsweep.

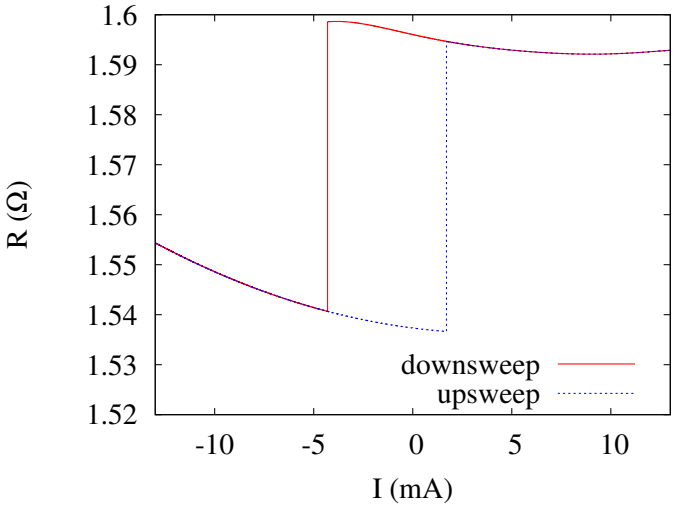


Figure 3.18: Reconstructed resistance of the spin valve after Albert *et al.* [147]. First, the voltage drop over the spin valve is determined by integrating the fit functions for the differential resistance. The results are then divided by the applied current.

Dimensioning of the circuit

The circuit consists of an input stage, two transistor switches, which are driven by the signal from the input stage, and an output stage. All sub-circuits will be described in the following.

Input stage. The input stage of the circuit is a non-inverting Schmitt trigger consisting of the resistors R_1, R_2 and the operational amplifier X_1. A Schmitt trigger is a comparator with two different switching points [167]. Let U_+ be the positive supply voltage of X_1 and U_- its negative supply voltage. The output voltage of the Schmitt trigger, U_H, shows a rectangular-shaped hysteresis and can attain two values, either U_+ or U_-. Depending on the choice of R_1, R_2, and the supply voltages of the operational amplifier the switching points U_C^+ and U_C^- can be set. U_C^+ denotes the switching point where U_H switches from U_- to U_+ and similarly U_C^- denotes the switching point where U_H switches from U_+ to U_-. For a non-inverting Schmitt trigger U_C^+ reads as

$$U_C^+ = -\frac{R_1}{R_2} \cdot U_-. \tag{3.34}$$

Similarly U_C^- reads as

$$U_C^- = -\frac{R_1}{R_2} \cdot U_+. \tag{3.35}$$

In order to obtain $U_C^- = -4.3$ V and $U_C^+ = +1.7$ V choosing $R_1 = 1.7$ kΩ and $R_2 = 10$ kΩ yields $U_- = -10$ V as well as $U_+ = 25.295$ V. Figure 3.19 shows the circuit diagram of the input stage.

To ensure a proper operation of the Schmitt trigger the input voltage always has to be less than the positive supply voltage U_+ of the operational amplifier and larger than its negative supply voltage U_-. Particular attention should be given to the situation when one of the switching points is quite close to 0 V while the other is not. For a large range of the input voltage, a large positive supply voltage and a small negative supply voltage are required. From Eqs. 3.34 and 3.35 it follows that

$$U_- = \frac{U_C^+}{U_C^-} \cdot U_+. \tag{3.36}$$

To solve this equation, one of the supply voltages has to be chosen a priori, for example U_+. If U_C^- is closer to 0 V than U_C^+, $|U_C^-| < |U_C^+|$ holds. In this situation $|U_-| > |U_+|$ applies, however $|U_-| = |U_+|$ would be desirable. If one of the switching points is close to 0 V, it limits the possible range for the input voltage, since a switching point close to 0 V results in a large supply voltage.

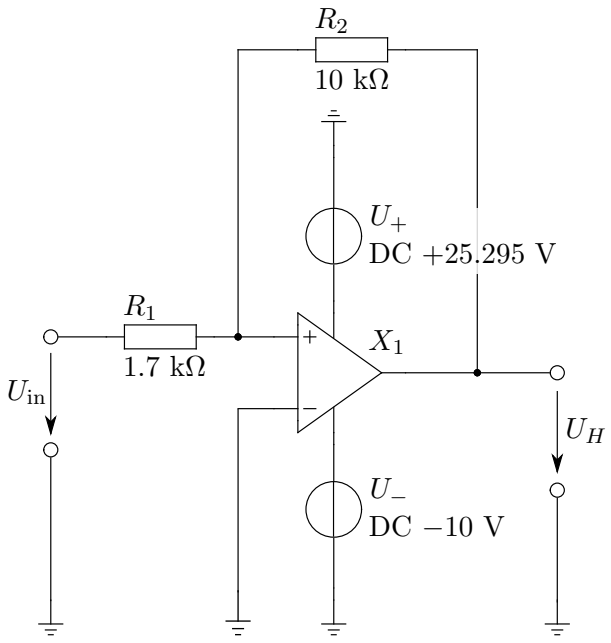


Figure 3.19: Circuit diagram of the input stage of the circuit. The input signal U_{in} corresponds to the current that is required to switch the resistance of the spin valve. U_+ is the positive supply voltage of the operational amplifier X_1 and U_- is its negative supply voltage. Together with the resistors R_1 and R_2 the switching points can be set. For the simulations the LM8261 operational amplifier from National Semiconductor was used. For this operational amplifier the input voltages of the circuit are within the range specified by the supply voltages (at least ±2.5 V and at most ±30 V) [203]. U_H is the output voltage of the Schmitt trigger; it can attain two values. With the given values the output voltage switches from U_- to U_+ at an input voltage $U_{\text{in}} = 1.7$ V. At input voltages less than $U_{\text{in}} = -4.3$ V the output voltage becomes U_-.

Transistor switches. The Schmitt trigger provides an output voltage U_H which can attain two possible values (see previous subsection). The value of U_H corresponds to either the upper or to the low resistance state. This signal controls the gate voltage of an n-channel field-effect transistor M_1 and that of a p-channel field-effect transistor M_2. Hence, depending on the state of U_H always one transistor is conductive, whereas the other transistor is turned off. Because the steps in the hysteresis curve are not modeled within the corresponding fit function, one has to overlay the voltages that represent the low- and high-resistance states. If one suppresses the voltage that corresponds to the high-resistance state in the low-resistance mode of the circuit and accordingly the voltage for the low-resistance state in the high-resistance mode, the hysteresis curve is reconstructed. Both fit functions are defined in the same range of input voltage. The switching between both modes is performed by the input stage (cf. Fig. 3.19). As can be seen from Fig. 3.20 and Fig. 3.22 the transistor M_1 forms a voltage divider with the resistor R_5 over which the voltage between the voltage-controlled voltage source B_1 and ground drops. The output is the voltage at the node between R_5 and M_1 (denoted as a in Fig. 3.20) and ground. The voltage of B_1 depends on the input signal U_{in} and is expressed in terms of an equation, which can be found in the appendix A.5. The voltage of B_1 corresponds to the high-resistance state that was constructed from the hysteresis curve. If the transistor is conductive it has a low resistance compared to the resistor R_5. In this situation the voltage from B_1 completely drops over R_5. U_H is then equal to U_+; the resistance of the spin valve is at its high level. If U_H is equal to U_- the voltage between R_5 and M_1 has almost vanished[9]. This configuration corresponds to the low-resistance state of the spin valve. Now the signal from B_1 is completely suppressed. The voltage divider formed by M_2 and R_8 can be explained similarly. Here the output voltage drops between the node b and ground. The signal from B_2 corresponds to the low-resistance state of the hysteresis curve. Consequently, when reconstructing the hysteresis curve at the output stage, one has to take the sum between the upper- and low-resistance state. Both transistor switches are shown in Fig. 3.20 and Fig. 3.22 respectively.

For proper operation the resistance of each transistor should be linear when it is conductive. This holds if the transistor is operated in its triode mode. The drain-source current I_{DS} for M_1 and M_2 amounts to

$$I_{\text{DS}} = K \cdot U_{\text{DS}} \left(U_{\text{G}} - U_{\text{TH}} - \frac{U_{\text{DS}}}{2} \right), \tag{3.37}$$

where K is the transconductance parameter, U_{DS} is the applied drain-source voltage, U_{G} is the voltage between gate and ground, and U_{TH} is the threshold voltage [167]. The channel-length modulation is neglected. The resistance of the transistor in its on-state, R_{on}, depends on the current across the transistor's channel and the applied drain-source voltage. From

[9] The resistance of a transistor that is switched off can be determined with a Wheatstone bridge (cf. Fig. 3.2 on page 40). The resistance of a transistor was found to be in the order of 1 TΩ when the transistor was switched off.

Eq. 3.37 it follows that

$$R_{\mathrm{on}} = \frac{1}{K \cdot \left(U_{\mathrm{G}} - U_{\mathrm{TH}} - \frac{U_{\mathrm{DS}}}{2} \right)}. \tag{3.38}$$

In contrast to an Ohmic resistor, in Eq. 3.38 the resistance still depends on U_{DS}. The on-resistance of both transistors is linearized with a superposition of a control voltage with the respective drain-source voltage at the gate terminal [167]. As can be seen in Fig. 3.20 and Fig. 3.22 the linearization is achieved with the resistors R_3 and R_4 for the n-channel transistor and with R_6 and R_7 for the p-channel transistor. The control voltage is U_H. Each of the resistors is chosen to be 1 MΩ in order to prevent current flowing elsewhere than from the drain to the source of the respective transistor. The gate voltage U_G is the voltage between gate and ground

$$U_G = \frac{B_1 + U_H}{2}. \tag{3.39}$$

A similar equation for M_2 can be obtained by replacing B_1 with B_2. Both are non-linear voltage-controlled voltage sources that represent the resistance states of the spin valve. By default, in NGSPICE's Shichman-Hodges model the channel-length modulation is disabled. It follows that the resistance of each transistor in its on-state can now be written as

$$R_{\mathrm{on}} = \frac{1}{K \cdot (\frac{U_H}{2} - U_{\mathrm{TH}})}, \tag{3.40}$$

where K is the transconductance parameter and U_{TH} the threshold voltage of the respective transistor. The voltage B_1 (and B_2 respectively) correspond to U_{DS}. The choice of K and U_{TH} is arbitrary[10]. The actual choice however must ensure that $R_{\mathrm{on}} \ll R_5$ and $R_{\mathrm{on}} \ll R_8$. For the simulations $K = 2.255\ \mathrm{A/V^2}$ and $U_{\mathrm{TH}} = 1\ \mathrm{V}$ for the n-channel transistor as well as $K = 2.255\ \mathrm{A/V^2}$ and $U_{\mathrm{TH}} = -1\ \mathrm{V}$ for the p-channel transistor were used.

The parameters yield an on-resistance $R_{\mathrm{on,n}} \approx 0.0380\ \Omega$ for the n-channel transistor M_1. Figure 3.21 shows the on-resistance of M_1 if a voltage $U_H = 25.259\ \mathrm{V}$ is applied.

The on-resistance of the p-channel transistor M_2 amounts to $R_{\mathrm{on,p}} \approx 0.1109\ \Omega$. Figure 3.23 shows the on-resistance of M_2 if a voltage $U_H = -10\ \mathrm{V}$ is applied. Both values for the on-resistances of M_1 and M_2 are comparatively small compared to R_5 and R_8.

[10] This statement is valid as long as the circuit is not to be assembled with real components on a printed circuit board.

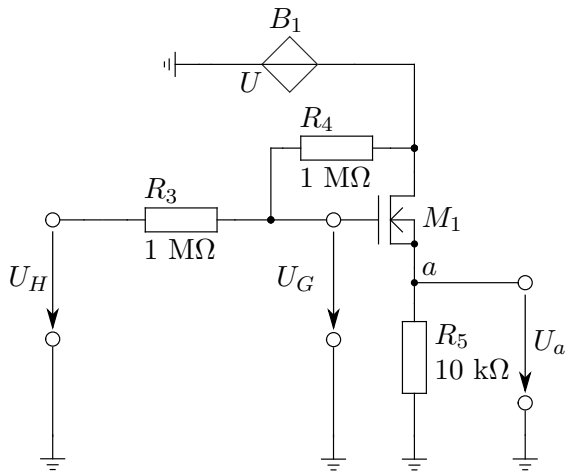


Figure 3.20: Circuit diagram of a transistor switch based on a voltage divider with variable load. U_H is the output voltage of the input stage (cf. Fig. 3.19). It can attain two values, U_- or U_+. If $U_H = U_-$ holds then M_1 is turned off. That means the voltage U_a between the nodes a and ground is zero and the voltage from the source B_1 is completely suppressed. B_1 generates a voltage that corresponds to the high resistance state of the hysteresis curve. If $U_H = U_+$ the transistor M_1 is conductive. The resistors R_3 and R_4 linearize the resistance of M_1 in its on-state. For M_1 the standard parameters of NGSPICE's Shichman-Hodges model were used, except for the threshold voltage `VTO` = 1 V and the transconductance parameter `KP` = 2.255 A/V^2. The source terminal and the bulk terminal of the transistor M_1 are shorted.

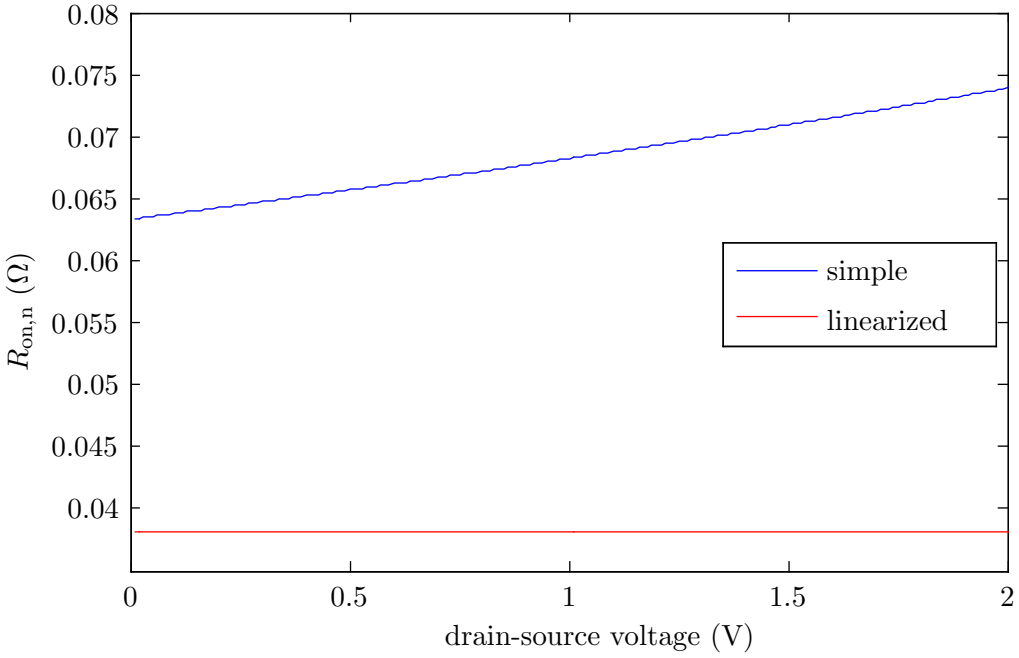


Figure 3.21: Comparison of the linearized on-resistance $R_{\mathrm{on,n}}$ of transistor M_1 with $R_3 = R_4 = 1$ MΩ (red) and without R_3 and R_4 (blue). The circuit is shown in Fig. 3.20. For M_1 the standard parameters of NGSPICE's Shichman-Hodges model were used, except for the threshold voltage `VTO` = 1 V and the transconductance parameter `KP` = 2.255 A/V^2. The source terminal and the bulk terminal of the transistor M_1 were shorted; $U_H = 25.259$ V. The resistances were simulated. The simulated linearized resistance is in good agreement with the calculated value (cf. Eq. 3.40).

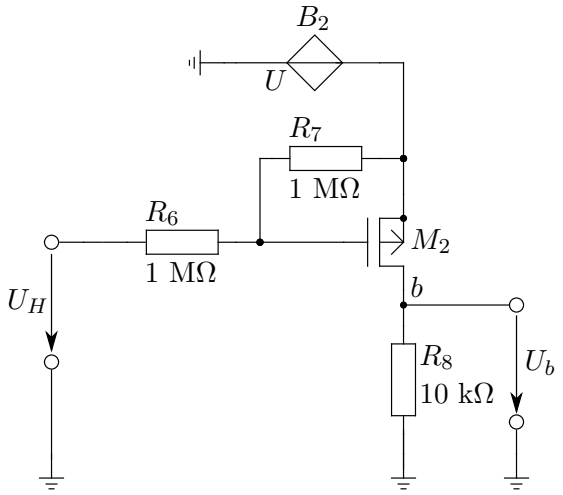


Figure 3.22: Circuit diagram of a transistor switch based on a voltage divider with variable load. U_H is the output voltage of the input stage (cf. Fig. 3.19). It can attain two values, U_- or U_+. If $U_H = U_-$ holds then M_2 is conductive. The voltage U_b between the node b and ground corresponds to the present value of B_2. B_2 generates a voltage that corresponds to the low resistance state of the hysteresis curve. If $U_H = U_+$ the transistor M_2 has a high resistance. Between the nodes b and ground the voltage from B_2 is suppressed. The resistors R_6 and R_7 linearize the resistance of M_2 in its on state. For M_2 the standard parameters of NGSPICE's Shichman-Hodges model were used, except for the threshold voltage `VTO` $= -1$ V and the transconductance parameter `KP` $= 2.255$ A/V^2. The drain terminal and the bulk terminal of the transistor M_2 are shorted.

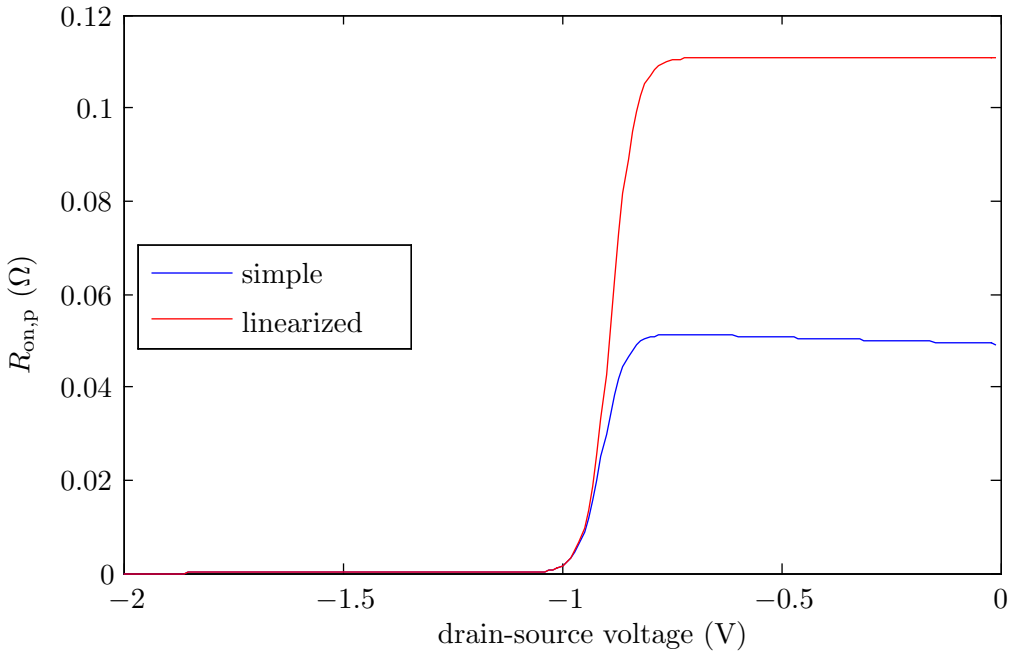


Figure 3.23: Comparison of the linearized on-resistance $R_{\mathrm{on,p}}$ of transistor M_2 with $R_6 = R_7 = 1$ MΩ (red) and without R_6 and R_7 (blue). The circuit is shown in Fig. 3.22. For M_2 the standard parameters of NGSPICE's Shichman-Hodges model were used, except for the threshold voltage `VTO` $= -1$ V and the transconductance parameter `KP` $= 2.255$ A/V^2. The drain terminal and the bulk terminal of the transistor M_2 were shorted; $U_H = -10$ V. The resistances were simulated. The origin of the step in both graphs remains unclear. For drain-source voltages greater than -1 V the simulated linearized resistance is in good agreement with the calculated value. The impact of the step on the functionality of the voltage divider formed by M_2 and R_8 is negligible, because in each graph (i) both values for the resistance are still very small compared to R_8 and (ii) the drain-source voltage in the spin-valve circuit lies in the range of some mV. In this case the on-resistance is linear to a good approximation.

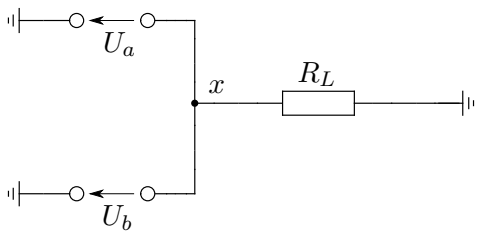


Figure 3.24: Circuit diagram of the output stage of the spin-valve circuit. The voltages U_a and U_b are the outputs of the transistor switches, see Figs. 3.20 and 3.22. At the node x both voltages are superposed. The resistor R_L is the load of the output stage.

Output stage. If the node between M_1 and R_5 is denoted as a and the node between M_2 and R_8 as b, the output voltage of the circuit is the sum of the voltages

$$U_{\text{out}} = U_a + U_b. \tag{3.41}$$

The sum of U_a and U_b can be obtained with the output stage shown in Fig. 3.24 taking into account a load R_L.

A compact model is characterized through the trade-off between the accuracy of the results from simulations with the model and the complexity of the computation. There are three goals to be achieved with the design of the circuit.

1. The load of the circuit should have little influence on the circuit's output voltage.
2. The circuit should consist of as few components as possible.
3. There should be no restrictions with respect to the fit functions for the low- and high-resistance state.

Insensitivity against loads. The output voltage is the sum of the voltages for the high-resistance and low-resistance branch. Simulations were performed for different values of R_L. In Fig. 3.25 the hysteresis of the circuit is shown for a load of 1 GΩ.

The output voltage of the circuit represents the electrical resistance of a spin valve. A dependency of the output voltage on the circuit's load falsely implies that the resistance of the spin valve would depend on another resistor connected to it. Instead, the output voltage must be insensitive to loads. The output stage of the circuit is shown in Fig. 3.24. The resistor R_L is the load of the circuit; it acts as a pull-down resistor. Figure 3.26 shows the difference between the reference voltage at a load of 1 GΩ and the output voltages at a load of 100 Ω. For the up- and downsweep the difference lies in the order of µV.

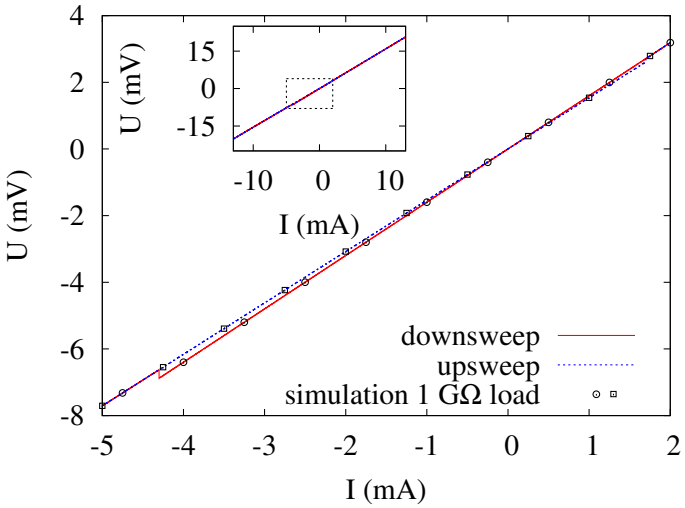


Figure 3.25: Output voltage of the spin-valve circuit if a spin valve after Albert *et al.* (Ref. [147]) is mimicked. The output voltage is the sum of the voltages that represent the high resistance and low resistance branch. The ⊙ symbols denote the results from a simulation with 1 GΩ load for the downsweep; the ⊡ symbols stand for the simulation of the upsweep with the same load. The blue dashed line is the integrated differential resistance during the upweep and the solid red line is the integrated differential resistance during the downsweep. See the appendix A.5 for the fit functions.

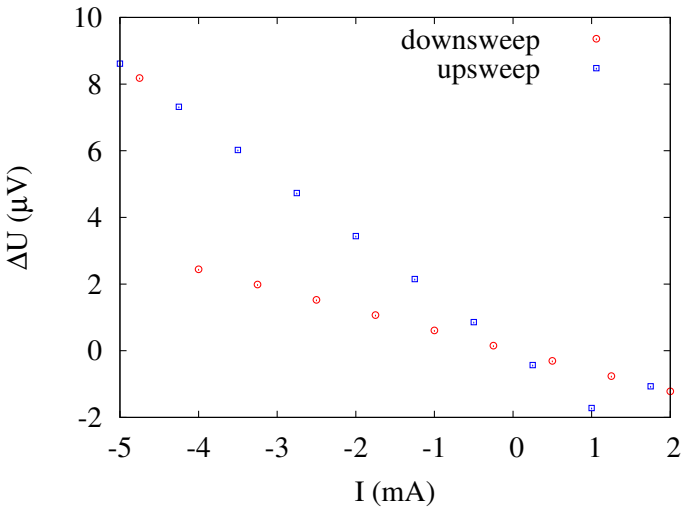


Figure 3.26: Voltage difference between the output voltage at a load of 100 Ω and the output voltage at a load of 1 GΩ. From the voltage with load 100 Ω, the voltage at 1 GΩ load was subtracted.

Simplicity. In order to ensure the convergence of a simulation the circuit should consist of as few components as possible. Mukherjee and Kurinec address the problem of convergence of simulations in the context of their proposal for a circuit mimicking spin valves [5]. They identify operational amplifiers as the main source of convergence-related problems. Yet Mukherjee and Kurinec do not analyze the converge in depth. If one neglects the actual implementation of the Schmitt trigger, that is, the implementation of the operational amplifier, the circuit described here is simpler than the one by Mukherjee and Kurinec. It only consists of 11 resistors, 8 voltage sources, and 2 transistors compared to 24 voltage and current sources, 18 resistors, and 6 diodes. The complexity of the circuit can surely be reduced further by using a simpler implementation of the operational amplifier, similar to Mukherjee and Kurinec's idea. A detailed analysis of the complexity of Mukherjee and Kurinec's circuit and the circuit presented here has not yet been performed (cf. the Outlook on page 85).

Flexibility. The non-linear voltage-controlled voltage sources B_1 and B_2 implement the low and high resistance state of the hysteresis curve. These voltage sources allow one to employ the best suited fit function for low resistance state and high resistance state and thus full flexibility of the design. In comparison to the recent work by Lee *et al.* this is an asset; the authors make use of a similar approach for the high resistance state of a hysteresis only [184].

Figure 3.27 shows the circuit completely. As discussed above circuit is insensitive to loads, simple in its assembly and flexible. The accuracy of its output voltage is tunable with respect to measured reference data. In the circuit the spin valve's resistance is expressed in terms of the corresponding voltage drop. Simulations proved that the output voltage is almost independent of the circuit's load (see Fig. 3.26). The circuit is simpler than the circuits described in other recent publications on the subject [5] and more flexible [184]. For the circuit the input signal, which is the current I_{in}, is mapped onto a voltage U_{in}. The mapping function is Ohm's law $U_{\text{in}} = R_{\text{conv}} \cdot I_{\text{in}}$ where U_{in} is the input voltage to the circuit, R_{conv} is the resistance for conversion, and I_{in} is the current applied to the spin valve. R_{conv} was chosen to be 1 kΩ[11]. In the simulations the conversion is achieved through a linear current-controlled voltage source (see the netlist in appendix A.6). A common way to achieve the conversion in a real circuit is to use an operational amplifier [199]. The micromagnetic simulation of a spin valve can be very resource-demanding. The smallest length scale which determines the resolution of the spatial discretization in a ferromagnetic structure is the *exchange length* l_{ex}; it is 3.9 nm for iron [140]. The time resolution lies below the ps-regime. Several publications show that the magnetization of the free layer oscillates in the range of some GHz when the spin valve is excited [85, 207, 208]. A time resolution of some ns is thus not sufficient to resolve the dynamics appropriately. Recently the switching time in a current-driven MRAM cell was measured to be 100 ps [209]. In comparison to the micromagnetic simulation of a spin valve, the simulation via an equivalent electrical circuit shows a drastic reduction of the complexity. Depending on the application one can use different circuits with different levels

[11] This value was used in the simulations. In principle, any value $R_{\text{conv}} = U_{\text{conv}}/I_{\text{conv}}$ is possible. The only limitation here is the maximum and minimal input voltage for the operational amplifier.

of accuracy. The circuit discussed above matches some of the quality criteria for compact models (cf. Ref. [172]):

- A quality model captures all relevant effects of the device. At present, the circuit mimics only the most important property, the hysteresis of the electrical resistance. The circuit however could be modified in order to incorporate other properties of a spin valve, like the oscillation of the magnetization of the free layer.
- The circuit is predictive at a high degree of accuracy. The accuracy of the circuit can be tuned with the choice of the fit functions for both branches.
- The circuit is flexible and can be adapted to given experimental reference data.
- The model in terms of the functions for lower and upper branch does not contain integrals, differentials or derivatives.
- The circuit provides a means to gain new insights into the function, performance characteristics, or limits of systems based on spin valves.
- In contrast to a micromagnetic simulation the circuit is an approach to increase the efficiency of the simulation results without loss of accuracy.

In contrast to the circuit for a rectangular-shaped hysteresis (cf. Sec. 3.1), the circuit from above possesses two terminals. The input voltage U_{in} (cf. Fig. 3.19 or Fig. 3.27) is applied at the IN terminal and ground. The output voltage drops between the node x and the reference potential, comparable with an Ohmic resistor. Dividing the output voltage of the circuit by the input current yields the resistance of the spin valve. The calculated resistance is shown in Fig. 3.18 and the simulated resistance in Fig. 3.28.

Feasibility of logic gates

There are no fundamental objections about setting up a logic gate with the aforementioned circuit (e.g. employing Richter's concept [114]). With the circuit the spin valve is modeled as a current-controlled voltage source. In contrast to the circuit in Sec. 3.1 the spin valve is modeled as a device with two terminals, one input signal will generate the output signal. This design implies that the resistance of the spin valve can never be programmed and sensed at the same time. For its use in a logic gate the circuit has got to be extended such that programming and sensing are possible simultaneously. If the resistance is sensed, the programming signal must be set to zero at the same time. That implies that an extra control signal must be introduced to the circuit. The control signal may be denoted as "write enable". If writing is enabled via this signal, the programming voltage is passed to the input of the Schmitt trigger while the voltage for sensing is disabled. If writing is suppressed though, the sensing voltage must be passed to the Schmitt trigger instead. In digital electronics, a switch is commonly implemented with a field-effect transistor. Both, n-channel or p-channel transistors may be employed for that purpose. Figure 3.29 shows a digital switch on the basis of an n-channel transistor. The transistor shown there can be considered as the series of two diodes, the

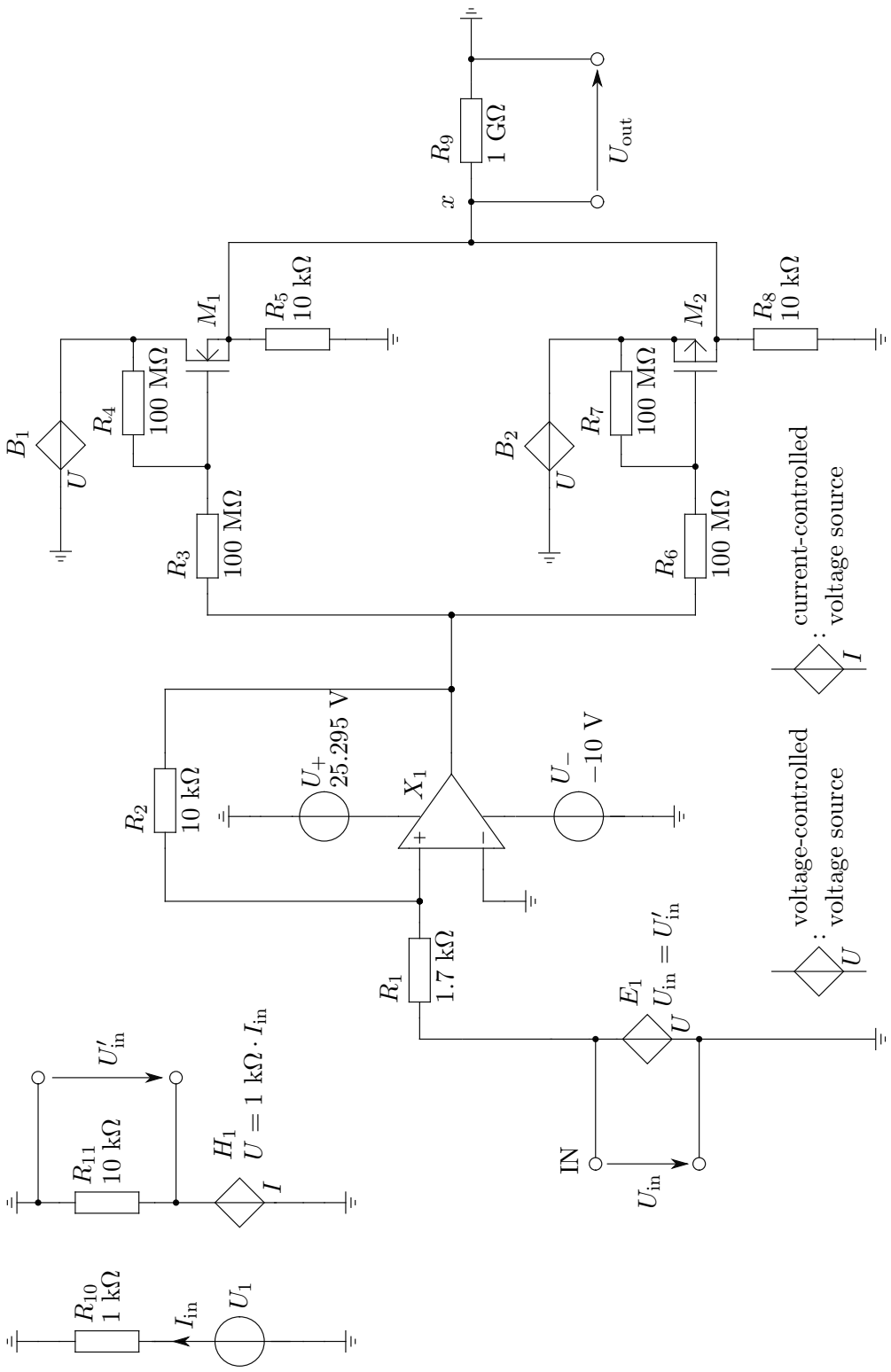


Figure 3.27: Complete diagram of the circuit for realistically mimicking the hysteresis curve of a spin valve. The figure combines the sub-circuits from Fig. 3.19, Fig. 3.20, Fig. 3.22, and Fig. 3.24.

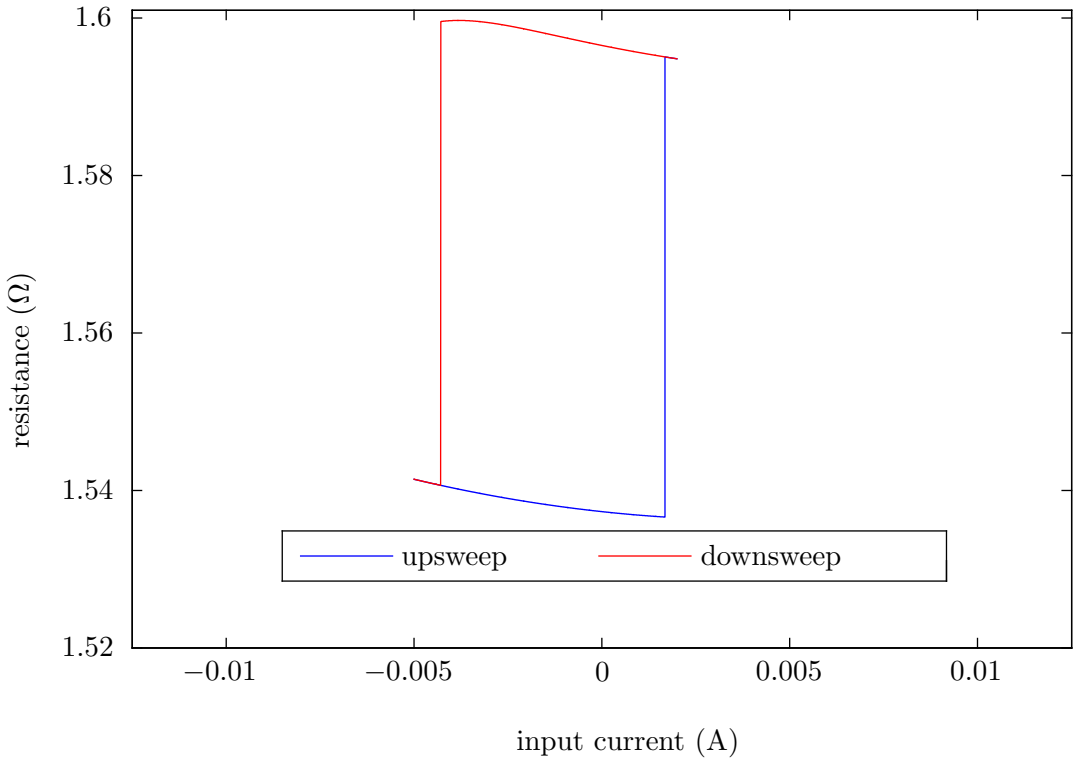


Figure 3.28: Simulated resistance of the spin-valve circuit mimicking a spin valve after Albert *et al.* [147] at a load of 1 GΩ.

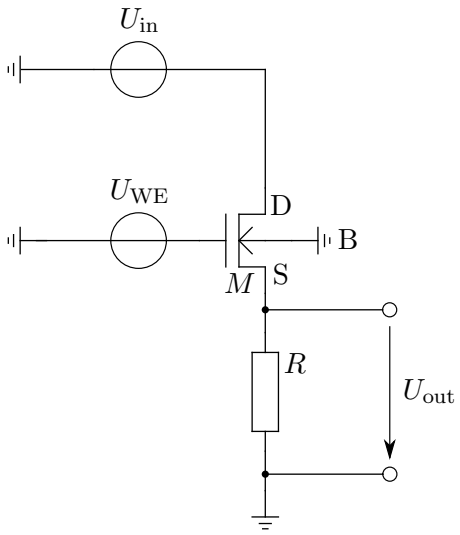


Figure 3.29: Circuit diagram of a transistor switch. The input voltage U_{in} drops over the resistor R as the output voltage U_{out} if the transistor M is switched on (in this case U_{WE} is above the transistor's threshold voltage). If switched off, the transistor represses the input voltage, and the output voltage is 0 V. The drain, the bulk, and the source of the transistor are denoted as D, B, and S, respectively. The resistor R acts as a pull-down resistor.

drain-bulk diode and the source-bulk diode. Due to the symmetry of drain and source in the transistor, the polarity of the applied drain-source voltage can be either positive or negative. For proper operation of the switch it is important to operate one of these diodes in forward direction (or short circuited), and the other diode in reverse direction[12].

In a common set-up of a switch based on an n-channel field-effect transistor source and bulk are short circuited. In this case the applied voltage between drain and source must possess positive polarity. For a negative drain-source voltage in turn the drain-bulk diode could be short circuited (cf. Figs. 3.20 and 3.22). Here a p-channel field-effect transistor is operated with a positive drain-source voltage. The circuit in Fig. 3.29 can already be considered a transmission gate. In the literature a transmission gate consists of an n-channel transistor in series with a p-channel transistor and an inverter for generating the gate voltage of the p-channel transistor from the "write enable" voltage (that serves as the gate voltage for the n-channel transistor) [201, 210]. By introducing a transmission gate the spin-valve circuit is transformed into a component with three terminals. Similarly a transmission gate can also be added to the circuit for mimicking an idealized, rectangular-shaped hysteresis (see Sec. 3.1) to mimic current-driven switching of a spin valve more realistically. If the applied drain-source voltage changes its polarity, the switch and the classical transmission gate can-

[12]The term "proper operation" in this context stands for a current flow through the channel when the transistor is switched on. If the drain-bulk diode and the source-bulk diode would be forward-biased, drain and source would be connected to a negative potential and hence no current would flow. If both would be reverse-biased, also no current could flow through the channel between drain and source.

not be applied. Unfortunately exactly this situation occurs with the programming signal of a spin valve. Otherwise the spin valve could not store data nonvolatile. In his Diploma thesis Tobias Kipp (Research group Computer Engineering, Universty of Hamburg) solved this problem. His solution is a modified transmission gate. The circuit is described in Ref. [205]. Kipp's circuit consists of twelve field-effect transistors. It should be investigated in which way the transmission gate could be optimized. It should also be studied if the sensing and programming mode can be implemented through adjusting the shape of the signal from the input voltage sources directly, similar to the current-to-voltage conversion in the spin-valve circuit[13].

If the resistance is reproduced at such a high level of accuracy, it is necessary to select operating points. The range of current for which data of the measured resistance is available determines the possible range for the input signal in a simulation. Beyond the range where data is provided, no valid assumption can be made about the resistance of the spin valve.

The work by Kawahara *et al.* provides no accurate data of the spin valve's resistance (cf. Fig. 3.6 and Fig. 3.7). Therefore it is not possible at the moment to determine adequate fitting functions for the hysteresis of Kawahara's spin valve.

[13]The conversion from current to voltage for the input signal of the spin-valve circuit is achieved by a combination of a voltage-controlled current source (to generate the input current first) and a current-controlled voltage source (which performs the actual conversion).

Chapter 4

Conclusion and outlook

Conclusion

There are two strategies to raise the number of computations per time step; first, by enhancing the computer's architecture. In this field it is investigated for example how the redundancy of a computation can be reduced. In a von-Neumann computer each instruction is decoded prior to the execution of the instruction (meaning the hardware is programmed according to the demands of the instruction). Decoding is repeated, even when one and the same instruction is repeated many times in a row. Reducing the time where components of the computer are idle or parallel processing of data are other useful techniques for speeding up the computer. Today computer architecture is an active and important field of research as the examples for new innovative architectures indicate.

The performance of a computer can be increased on the other hand through improvements of the technologies to implement its components. The most prominent example is the miniaturization of these components. Gordon Moore had observed that along with miniaturization the cost of a chip decreased. With miniaturization scientists will have to face challenges in the future. These affect nearly all aspects of an integrated circuit. With a simple example a fundamental limit was estimated. Assuming the current technology node and that Moore's law is kept valid in the future, by 2021 structures would be as small as the lattice constant of silicon. It can be doubted if devices of this size will still work properly. Traditional, or in other words baseline technologies for logic and memory devices are based on field-effect transistors made with semiconductor materials. Even with miniaturization, the traditional technologies still show principle drawbacks. Static random-access (SRAM) memory cells store data volatile and consist of eight transistors. In dynamic random-access memory (DRAM) cells the data is represented through the charge of a capacitor; a periodic refresh of the charge is required in order to maintain the stored data. Flash memory is a nonvolatile memory technology. It however exhibits a comparatively small number of write cycles (in contrast to SRAM for example) until the memory cell becomes unreliable. In the context of this thesis the improvements of a technology were denoted as scaling. Scaling can weaken a technology's disadvantages. For example decreasing the area for one SRAM cell by scaling down the

dimensions of a transistor weakens the disadvantage that a single cell still consists of eight transistors. In order to maintain the performance gain of logic and memory devices in light of the limits of miniaturization, alternative technologies could be employed. The International Technology Roadmap for Semiconductors is a summary of the state-of-the-art in fabrication of logic and memory devices [24, 33, 51]. It allows for assessment of the feasibility of future devices, that is, devices made of the baseline technologies as well as devices made with alternative technologies. A couple of alternative technologies are listed in the ITRS and were introduced in this thesis.

Among these emerging alternative technologies are many magnetic devices and in particular spin valves; they are ferromagnetic structures of nanometers in size. Their electrical resistance can be tuned by either an electrical current or a magnetic field. Spin valves are a promising novel technology that overcome the principle drawbacks of the baseline technologies. There are as well challenges, for example concerning the miniaturization of spin valves, but spin valves store data nonvolatile and only one spin valve is required per bit. In comparison to Flash memory, spin valves bear a billion times more write cycles. It was pointed out that spin valves are universal devices. Besides their use in memory devices, they can also be used as high-frequency oscillators or for logic gates and are particularly well suited for outer space applications due to their radiation hardness. Many works on logic gates based on spin valves propose the combination of spin valves with semiconductor field-effect transistors.

Simulation of electrical circuits has become an important tool for research and design. If complex systems (consisting of many devices) are to be simulated, it is essential that the device models reflect the relevant properties efficiently. The basic level for system design in Gajski and Kuhn's Y chart is the circuit level. For circuit design compact device models are essential. The compact model of a device is a trade-off between the accuracy of the model (in comparison with experimental data) and the complexity of the computation when employing this model. The most accurate model for the description of spin valves is the Landau-Lifshitz-Gilbert equation, but this model cannot be considered as a compact model. First, it does not satisfy criteria for compact models and second, the Landau-Lifshitz-Gilbert equation does not allow to compute the electrical properties of a spin valve (e.g. the resistance) directly. The state-of-the-art of compact models for spin valves was reviewed. It was found that most of the existing models are tailored to magnetic tunnel junctions. A more flexible approach, which could even be applied to devices beyond spin valves is using an equivalent electrical circuit. Such a circuit satisfies important quality criteria for compact models (e.g. the description of spin valve's behavior does not contain integrals or differentials) and makes spin valves accessible to circuit designers in their language. The assets and drawbacks of recent works on the topic were discussed. As a result, two new circuits mimicking spin valves were proposed in this thesis. First a circuit with as few components as possible was designed and evaluated (Publication "Spin Valves For Innovative Computing Devices And Architectures", Ref. [196], and its supplementary material on page 35 et seqq.). The circuit is approximating the hysteresis of a spin valve's resistance. Yet, it already yields reasonable predictions of a

spin valve's performance. In two case studies the performance of spin valves in logic gates was investigated. From experimental findings it is assumed that the resistance of a spin valve can attain two values, high or low resistance. On the basis of the case studies it was found that the difference between the resistance states is relevant for proper operation of the logic gate as expected. Astonishingly the voltage applied to the spin valve for measuring the resistance plays an even more dominant role. It was pointed out that additional circuitry is inevitable if the gate's output is intended to drive other gates. It needs to be investigated how this capability can be implemented efficiently. A simple solution is converting the gate's output with a comparator.

In Sec. 3.3 on page 64 et seqq. an equivalent electrical circuit was depicted that picks up the results from current publications (Lee *et al.* [184]; Mukherjee and Kurinec [5]) on the same topic and introduces enhancements. If a spin valve is modeled through a two-port network, the resistance cannot be programmed and measured independently from each other. A logic gate employing the latter circuit has not been investigated yet.

The circuits are not limited to spin valves only; similar devices showing a hysteresis can be modeled in terms of the circuit, e.g. ferroelectric random-access memory cells or phase-change memory.

Outlook

In the following several topics for further research are outlined.

Logic gates

Logic gates have been mimicked with the equivalent electrical circuit for a rectangular-shaped hysteresis only. Similarly logic gates can also be imitated with the second circuit (which allows mimicking the hysteresis precisely). Then a detailed analysis of the performance gain when using a rectangular-shaped hysteresis instead of an accurate hysteresis is possible. It could be investigated how much the complexity of the computation was reduced through the abstraction of the hysteresis curve. It could also be studied under which circumstances the accuracy of the hysteresis plays an important role for the predictability of the simulation.

Enhancement of the circuits

In terms of the circuit with a rectangular-shaped hysteresis curve, a current- and a field-driven spin valve differ only through the shape of the programming signal. For sensing the resistance of a current-driven spin valve, the programming signal must be set to zero. The obtained results are already reasonable, but the scheme of programming and sensing of a current-driven spin valve should be included in the circuit as soon as possible.

At present both circuits only reproduce the hysteresis of a spin valve's resistance. Both

circuits should be enhanced. An important feature of a spin valve is that the magnetization in the free layer is able to perform oscillations with frequencies in the order of some GHz. As experiments show, the oscillation is almost sinusoidal [85]. In a first approximation this feature could be implemented within the circuits through a sinusoidal voltage source. With an additional control signal it could be distinguished between the steady state hysteresis and the oscillator-like behavior of the spin valve. Furthermore, the temperature dependence of the hysteresis (or magnetization) should be considered. Lee *et al.* have proposed a solution already, however with a quite complicated circuit. It should be investigated if a simpler means for considering the temperature dependence of the magnetizations in the spin valve can be designed. Eventually thermally-assisted switching of spin valves could be included in the circuits. As Professor Dr. Hamid Vakilzadian from the University of Nebraska-Lincoln, USA, suggested, overloading of the spin valve should be studied. That means, it should be studied what happens to the shape of the output signal after a chain of spin valves.

Redesign of the operational amplifier

In the circuit for the rectangular-shaped hysteresis as well as in the circuit for mimicking a realistic hysteresis, models of real electronic components were used, for instance for an operational amplifier. This allows benefiting from the flexibility of real devices within the spin-valve circuit. For example asymmetrical supply voltages can be employed. Real components introduce parasitic effects to the spin-valve circuit. This affects for instance the clock frequency of the input signal. As a consequence a discrepancy between the circuit and the actual spin valve can arise. It is necessary to enhance the operational amplifier in order to study the behavior of spin valves that are clocked in the order of some GHz. Such high clock rates are demanded in today's computing systems. Another example for a deviation between reality and simulation is related to the range of the input signal. The possible range of the input for the circuit is determined by the supply voltages of the operational amplifier. Throughout this thesis, a current applied to a real spin valve was mapped onto an input voltage to the circuit. If the switching points of the original hysteresis are asymmetrical around the origin, the switching point closest to it determines the supply voltages (cf. the summary on page 50). An approach with full flexibility and no extra parasitic effects due to models of real components is desirable. Mukherjee and Kurinec identify the operational amplifier as the main source of convergence-related problems in a simulation [5]. This statement needs to be verified. In any case, a new design for the operational amplifier should reduce undesired effects on the circuit. In Ref. [210] Baker *et al.* depict a Schmitt trigger is that uses only six transistors. It should be investigated if this solution is applicable in the spin-valve circuits. An idealized operational amplifier would consist of three stages [211]: 1. a differential amplifier with high voltage gain, 2. a low-pass filter in order to prevent oscillations of the output voltage at high frequencies due to the high open-loop gain, and 3. an output buffer. The differential ampilfier can be implemented through a resistor if each input of the operational amplifier is connected to a terminal of the resistor. Yet, such a simple differential amplifier does not take into account the saturation of the output voltage (that depends on the supply voltages) in realistic devices.

Mathematical models for hysteresis

Another promising approach to get rid of the circuits' limitation in comparison to real spin valves are pure mathematical descriptions of the hysteresis which might even lead to an improved understanding of the underlying physics. A well-known model for the hysteresis was derived by Preisach already in 1935 [212,213]. Preisach's basic assumption is that a ferromagnet can be divided into magnetic domains, each switching between two different states. In the Preisach model the hysteresis for a single domain is a rectangular-shaped hysteresis curve with an upper switching point α and a lower switching point β. These elementary hysteresis loops are also denoted as *hysterons*. The hysteresis of the whole ferromagnet is the superposition of hysterons. Accordingly the model contains a weighting function $\mu(\alpha, \beta)$ that needs to be extracted for every hysteresis curve from experimental data. A important problem to be solved is that minor loops are required. Zirka and Moroz describe how to extract minor loops from a measured major loop because of symmetry considerations [214]. It could be subject to further research how to implement the Preisach model, that is, the synthesis of the weighting function $\mu(\alpha, \beta)$ in the circuits. The Preisach model is a phenomenological model since it does not give an explanation why the magnetization of a single domain switches when excited. The alternatives to the Preisach model are analytical models for hysteresis (e.g. Stoner-Wohlfarth model [139] and the Jiles-Atherton model [215]). They may also be considered for improvements of the circuits.

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Appendix A

Netlists of the circuits

The circuits whose design is described in the previous chapters were designed with the program `gschem`; this program is part of the gEDA toolkit [216]. It allows the circuit design with graphical symbols for each device. The graphical representation of the circuit is not compatible with NGSPICE[1], it comprises though all relevant information of a circuit. With the program `gnetlist` (also part of the gEDA toolkit) it is possible to translate the graphical representation into a netlist that NGSPICE understands. In the following the netlists for the equivalent circuit for mimicking spin valves, the Wheatstone bridge, and the logic gates (cf. Sec. 3.1 and Sec. 3.2) are listed.

A netlist represents the topology of the circuit. A netlist begins with a headline, which is ignored by the simulation program and terminates with a closing line (key word `.END`). Lines with comments start with `*`. A leading `+` indicates that the previous line continues. Each component of the circuit is specified within a line of the netlist. The definition of a component follows the assembly:

1. type (e.g. "R" for resistors,"C" for capacitors, "M" for field-effect transistors; voltage source are denoted with "V" and sub-circuits with "X".)
2. name (an alpha numeric string)
3. nodes of the component; the node `0` stands for ground
4. parameters of the component

Nodes are named with alpha numeric strings and are separated from each other by a space character. The number of components may vary depending on the model for the component; each parameter possesses a unique name. The assignment of a value to a parameter is expressed as `PARAM = value`. Some parameters are compulsory, while other are optional. If optional parameters are not specified explicitly, default values are assumed. For a detailed overview on the description of circuits in terms of netlists for SPICE and the analysis cf. Refs. [165, 180].

[1] NGSPICE is a precompiled open-source version of SPICE [217].

A.1 Netlist for the circuit for mimicking spin valves with rectangular hysteresis

Dimensioning of the circuit is described in Sec. 3.1. The operational amplifier is described in an extra model, which usually can be obtained from the manufacturer; the operational amplifier can be replaced by others according to one's own needs. Most manufacturers nowadays provide such models online. The netlist describes the upsweep of the input voltage. The circuit can conveniently be adopted to the downsweep by changing the line `.dc v1 -10 10 0.01` to `.dc v1 10 -10 -0.01`. Between the node `in` and `0` (ground) the input voltage drops. The output voltage drops over the node `out` and `0` (ground). The circuit is also shown in Fig. 3.1.

Start of code

```
* gnetlist -g spice-sdb -o ideal_spin_valve.net ideal_spin_valve.sch
************************************************************
* Spice file generated by gnetlist                         *
* spice-sdb version 4.28.2007 by SDB --                    *
* provides advanced spice netlisting capability.           *
* Documentation at http://www.brorson.com/gEDA/SPICE/      *
************************************************************
*==============  Begin SPICE netlist of main design ============

* include model for operational amplifier LM8261; file is located in the
* specified directory
.include /afs/physnet.uni-hamburg.de/users/grk1286/bguede/spice-models/
+ national_semi/lm8261/LM8261.MOD

* print voltages at the nodes "u_in", "u_hys", and "u_out" (batch mode)
.print tran u_in u_hys u_out

* input voltage (to generate the input signal)
Vin u_in 0 DC 1V

* the inverting Schmitt trigger
* the operational amplifier; the last entry in the line denotes the model
* name
X1 4 u_in 5 6 u_hys LM8261
R1 u_hys 4 4.8823k
R2 4 0 1k
* supply voltages for X1
* V2 is the positive supply voltage and V3 the negative
* supply voltage
V2 5 0 DC 10V
V3 6 0 DC -25.295V

* the resistors that linearize the resistance of the
* transistor
```

```
R4 2 u_out 100Meg
R3 u_hys 2 100Meg

* the transistor M1 with model definition
M1 u_out 2 1 1 mosfet
.MODEL mosfet NMOS (level=1 kp=2.255)

R6 0 u_out 1.59
R5 0 1 49

* the sensing voltage and the resistor that forms a voltage divider
* with the spin valve
Vsense 3 0 DC 5V
R7 u_out 3 1.59

* analysis (sweep the DC input signal from -10 V to +10 V in steps of 0.01 V)
.dc v1 -10 10 0.01

* end of netlist
.end
```

End of code

A.2 Netlist for the Wheatstone bridge for measuring the resistance of a field-effect transistor in its off-state

The Wheatstone bridge shown in Fig. 3.2 allows for the measurement of the resistance of the transistor M_1 when it is switched off.

Start of code

```
* gnetlist -g spice-sdb -o wheatstone.net wheatstone.sch
************************************************************
* Spice file generated by gnetlist                         *
* spice-sdb version 4.28.2007 by SDB --                    *
* provides advanced spice netlisting capability.           *
* Documentation at http://www.brorson.com/gEDA/SPICE/      *
************************************************************
*==============  Begin SPICE netlist of main design ============

* input voltage
V0 uin 0 DC 5V

* voltage divider for comparison
R8 uin a 1k
R9 a 0 1k

* transistor operated in off-state (operating point is set with
* the voltage at node "ugs" and the parameters in the transistor
* model NMOS)
```

```
20 M2 b ugs 0 0 mosfet
21 .MODEL mosfet NMOS (level=1 kp=2.255 vto=1)
22 V1 ugs 0 DC -11.3969V
23
24 * trimming resistor for M1
25 Roff uin b 0.996T
26
27 * print voltages at the nodes "uin", "a", and "b" (batch mode)
28 .print tran uin a b
29
30 * perform transient analysis (from 0 s to 60 ms in steps of 0.5 ms)
31 .tran 0.5m 60m
32
33 * end of netlist
34 .end
```

End of code

A.3 Netlist of the equivalent circuit for logic gates after Richter *et al.*

The logic gate is described in Sec. 3.2. The following netlist matches a spin valve similar to the measurement by Albert *et al.* [147]. The circuit is shown in Fig. 3.10. The output voltage is the difference between the voltages at the nodes `y` and `x`. The netlist for a single spin valve is included into the netlist for the gate via a sub-circuit. In SPICE / NGSPICE a sub-circuit is started with `.subckt` followed by its name and its nodes (inputs). The sub-circuit ends with `.ends`.

Start of code

```
1  * gnetlist -g spice-sdb -o nand-gate.net nand-gate.sch
2  ************************************************************
3  * Spice file generated by gnetlist                         *
4  * spice-sdb version 4.28.2007 by SDB --                    *
5  * provides advanced spice netlisting capability.           *
6  * Documentation at http://www.brorson.com/gEDA/SPICE/      *
7  ************************************************************
8
9  * sub-circuit for a single spin valve; a sub-circuit has its
10 * own namespace
11 * name: spin-valve
12 * terminals: 1. in, 2. sense, 3. out
13 .subckt spin-valve in sense out
14
15 X1 3 in 4 5 u_hys LM8261
16 V2 4 0 DC 10V
17 R6 out sense 1.59
18 R5 out 1 49
19 R4 2 sense 100Meg
20 R3 u_hys 2 100Meg
```

```
21 R2 u_hys 3 1k
22 R1 3 0 1k
23 M1 sense 2 1 1 mosfet
24 .MODEL mosfet NMOS (level=1 kp=2.255)
25 V3 5 0 DC -25.295V
26 .include /afs/physnet.uni-hamburg.de/users/grk1286/bguede/spice-models/
27 + national_semi/lm8261/LM8261.MOD
28 .ends
29
30 *==============  Begin SPICE netlist of main design ============
31 * include sub-circuit
32 .input spin-valve.lib
33
34 * print voltages at the nodes "y", reference branch, and
35 * "x", input branch (batch mode)
36 .print tran x y
37
38 * voltage divider for the input branch
39 V1 4 0 DC 5mV
40 R1 4 x 1.59
41
42 * inputs A and B for the logic gates (pulsed voltage sources)
43 V2 A 0 pulse -5 5 0 10u 10u 1m 2m
44 V3 B 0 pulse -5 5 0 10u 10u 2m 4m
45
46 * spin valves for the input branch; the model is "spin-valve"
47 X1 A x 1 spin-valve
48 X2 B 1 0 spin-valve
49
50 * voltage divider for the reference branch
51 V4 5 0 DC 5mV
52 R2 y 5 1.59
53
54 * programming of the reference branch (pulsed voltage sources)
55 V5 z1 0 pulse 5 -5 0 10u 10u 6m 12m
56 V6 3 0 pulse -5 5 0 10u 10u 6m 12m
57
58 * spin valves for the reference branch; the model is "spin-valve"
59 X3 z1 y 2 spin-valve
60 X4 3 2 0 spin-valve
61
62 * perform transient analysis (from 0 s to 4 ms in steps of 0.1 ms)
63 .tran 100u 4m
64
65 * end of netlist
66 .end
```

End of code

A.4 Netlist of the equivalent circuit for an Ohmic resistor

Start of code

```
* gnetlist -g spice-sdb -o resistor.net resistor.sch
************************************************************
* Spice file generated by gnetlist                         *
* spice-sdb version 4.28.2007 by SDB --                    *
* provides advanced spice netlisting capability.           *
* Documentation at http://www.brorson.com/gEDA/SPICE/      *
************************************************************
*==============  Begin SPICE netlist of main design ============
* Input voltage
V1 a 0 DC 1V

* Dummy voltage source for measuring the current
V2 b 0 DC 0V

* voltage-controlled current source
B1 a b I=v(a,b)/100

* plot results (batch mode)
.print dc a v2#branch

* perform dc sweep of the input voltage (from -5 V
* to +5 V in steps of 0.003 V)
.dc v1 -5 5 0.003

* end of netlist
.end
```

End of code

A.5 Fit-functions for the upper and lower branch of the spin valve's hysteresis after Albert *et al.*

The fit-function for the high resistance state is given by

$$\begin{aligned} f(x) = {} & 1.59653 - 0.0019282x \\ & + 0.000159941x^2 + 2.47928 \cdot 10^{-5}x^3 \\ & - 1.29323 \cdot 10^{-5}x^4 + 2.27943 \cdot 10^{-6}x^5 \\ & - 1.66664 \cdot 10^{-7}x^6 + 4.35218 \cdot 10^{-9}x^7, \end{aligned} \tag{A.1}$$

where it is assumed that the the original branch from the measurement has a domain of $I = [-4.3\ \text{mA}; 12.5\ \text{mA}]$, described in the equation by $x = 1\ \text{V}/1\ \text{mA}$. The variance of the residuals with respect to the data points is $1.65629 \cdot 10^{-7}$.

Correspondingly the fit-function for the low resistance state is assumed to have the domain

of $I = [-12.5\ \text{mA}; 1.75\ \text{mA}]$ and reads as

$$g(x) = 1.53734 - 0.00102197x + 0.000184457x^2, \tag{A.2}$$

where the domain is described by $x = 1\ \text{V}/1\ \text{mA}$. The variance of the residuals with respect to the data points is $1.12107 \cdot 10^{-7}$.

A.6 Netlist of the of circuit for a spin valve with a realistic hysteresis

The circuit can be adopted to the upsweep by changing the line `.dc v1 2 -5 -0.003` to `.dc v1 -5 2 0.003`. Between the node `in` and ground the input voltage drops. The output voltage drops over the node `out` and ground.

Start of code

```
* gnetlist -g spice-sdb -o rsv-downsweep.net rsv-downsweep_load-1giga.sch
************************************************************
* Spice file generated by gnetlist                         *
* spice-sdb version 4.28.2007 by SDB --                    *
* provides advanced spice netlisting capability.           *
* Documentation at http://www.brorson.com/gEDA/SPICE/      *
************************************************************
*==============  Begin SPICE netlist of main design ============

* gnetlist -g spice-sdb
+ real-sv-downsweep.sch

* The voltage source for DC sweep (in order to generate the current
* through the resistor)
V1 4 5 DC 0V
R10 5 0 1k

* SPICE cannot measure current directly, therefore it is measured through
* a voltage source (no voltage drop)
V0 4 0 DC 0V

* linear current-controlled voltage source conversion with a 1k resistor
H1 0 in v1 1k
R11 in 0 10k

* input voltage of the circuit; linear voltage-controlled voltage
* source (controlled with H1)
E1 x 0 in 0 1

** Schmitt trigger **

* model of LM8261
```

```
33 .include LM8261.MOD
34 R1 x 1 1.7k
35 R2 1 y 10k
36
37 * supply voltages
38 V2 2 0 DC 25.295V
39 V3 3 0 DC -10V
40 * op-amp
41 X1 1 0 2 3 y LM8261
42
43 ** transistor switches pt. 1 **
44
45 R3 y gate1 1Meg
46 R4 gate1 c 1Meg
47 R5 0 z 10k
48
49 * transistor model for M1 using the defaults of the LEVEL 1
50 * model except for kp and vto; shorted source and bulk
51 M1 c gate1 z z mosfet
52
53 * transistor model use defaults of LEVEL 1 except for kp and vto
54 .MODEL mosfet NMOS (level=1 kp=2.255 vto=1)
55
56 * controlled voltage source for implementing the fit-functions
57 * as voltages (high resistance state). The pre-factor 0.001 is due to the
58 * current to voltage conversion
59 B1 c 0 V=0.001*(1.59653*V(x)-9.641e-4*V(x)^2+5.33136667e-5*V(x)^3+6.1982e-6*V(x)^4
60 + -2.58646e-6*V(x)^5+3.79905e-7*V(x)^6-2.38091429e-8*V(x)^7
61 + +5.440225e-10*V(x)^8)
62
63 ** transistor switches pt. 2 **
64
65 R6 y gate2 1Meg
66 R7 gate2 d 1Meg
67 R8 0 z 10k
68
69 * transistor model for M2 using the defaults of the LEVEL 1 model except for kp
70 * and vto; shorted drain and bulk
71 M2 d gate2 z d mosfet2
72
73 * transistor model use defaults of LEVEL 1 except for kp and vto
74 .MODEL mosfet2 PMOS (level=1 kp=2.255 vto=-1)
75
76 * controlled voltage source for implementing the fit-functions
77 * as voltages (low resistance state). The pre-factor 0.001 is due to the
78 * current to voltage conversion
79 B2 d 0 V=0.001*(1.53734*V(x)-5.1485e-4*V(x)^2+6.14856667e-5*V(x)^3)
80
```

```
81 ** Output stage with load **
82
83 * load is 1 GOhm
84 R9 z 0 1g
85
86 * print the input current and output voltages in SPICE's batch mode
87 .print dc v0#branch z
88
89 * perform sweep from +2 V in steps of 0.003 V;  stop at -5 V (downsweep).
90 * For the upsweep begin at -5 V and stop at +2 V
91 .dc v1 2 -5 -0.003
92
93 * end of netlist
94 .end
```

End of code

Appendix B

Contributions to the manuscript "Spin Valves For Innovative Computing Devices And Architectures"

The work "Spin Valves For Innovative Computing Devices And Architectures" was presented at the 2008 Summer Computer Simulation Conference SCSC'08 (June 16-19, 2008, Edinburgh, United Kingdom) (Ref. [196]). In this paper the concept of a circuit is described, which mimics a spin valve whose resistance shows a rectangular-shaped hysteresis. Especially the dimensioning of the circuit is only briefly sketched in the paper. In Sec. 3.1 on page 36 et seqq. the final version of the circuit and its dimensioning to a given spin valve are depicted by means of two case studies. My own contributions to the paper are as follows:

- The abstract.
- The introduction. This section was written by myself together with Dr. Markus Bolte, and Professor Dr.-Ing. Dietmar P. F. Möller (Research group Computer Engineering, University of Hamburg) who all contributed equally.
- Sec. 2 "Theoretical considerations". This section was written by myself together with Benjamin Krüger (I. Institute for Theoretical Physics, University of Hamburg, Germany), Massoud Najafi, and Dr. Markus Bolte (Research group Computer Engineering, University of Hamburg); everyone contributed equally.
- The Sec. 3 "Prototype of an equivalent electronic circuit" until the beginning of Sec. 3.1 was authored by myself and Dr. Markus Bolte, Massoud Najafi, and Professor Dr.-Ing. Dietmar P. F. Möller, who all contributed equally.
- Sections 3.1-3.3.
- Sec. 4 "Summary and outlook".

Appendix C

Contributions to the manuscript "A Compact Model For Spin Valves in Computing Devices"

The text in Sec. 3.3 is based in parts on the manuscript "A Compact Model For Spin Valves in Computing Devices" (Ref. [206]) that is submitted for publication to IEEE Transactions on Circuits and Systems I: Regular Papers. The manuscript was written in cooperation with Benjamin Krüger (I. Institute for Theoretical Physics, University of Hamburg, Germany), Massoud Najafi, Tobias Kipp, Professor Dr.-Ing. Dietmar P. F. Möller (Research group Computer Engineering, University of Hamburg), and Dr. Scott Roy (Device Modelling Group, University of Glasgow, United Kingdom). My own contributions to the manuscript are as follows:

- The abstract.
- The introduction. This section was written by myself together with Massoud Najafi, Dr. Scott Roy, and Professor Dr.-Ing. Dietmar P. F. Möller who all contributed equally.
- The Sec. II "Physics of spin valves" was authored by myself with the help of Benjamin Krüger and Massoud Najafi. Both are experts in the field of micromagnetic simulations.
- The Sec. III "Design of the circuit". An extended version of the dimensioning can be found in Sec. 3.3 in this thesis. Benjamin Krüger, Massoud Najafi, and I discussed the fit functions (see appendix A.5 in this thesis).
- The results in Sec. IV. "Results" on the sensibility of the spin-valve circuit's output stage on loads were obtained by myself and Tobias Kipp who was a diploma student.
- Dr. Scott Roy and myself discussed intensely compact models. He suggested to study existent compact models for semiconductor devices (i.e. transistors and diodes) for my ferromagnetic spin valves.

- Professor Möller and myself worked out the structure of the manuscript.

Appendix D

Other publications / contributions to conferences

- B. Güde, M.-A. B. W. Bolte, B. Krüger, M. Najafi, and D. P. F. Möller, "Spin Valves For Innovative Computing Devices And Architectures", in *Proceedings of the 2008 Summer Computer Simulation Conference (SCSC'08)*, D. Cook and K. Taylor, Ed. San Diego, CA, USA: The Society for Modeling and Simulation, 2008, pp. 279–285.

- M. Najafi, B. Krüger, S. Bohlens, G. Selke, B. Güde, M. Bolte, and D. P. F. Möller, "The micromagnetic modeling and simulation kit M^3S for the simulation of the dynamic response of ferromagnets to electric currents", in *Proceedings of the 2008 Grand Challenges in Modeling and Simulation Conference (GCSM'08)*, H. Vakilzadian, R. Huntsinger, T. Ericson, and R. Crosbie, Eds. San Diego, CA, USA: The Society for Modeling and Simulation, 2008, pp. 427–434.

- M. Najafi, G. Selke, B. Krüger, B. Güde, B. Krause-Kyora, M. Bolte, G. Meier, and D. P. F. Möller, "A Case Study for the Parallelization of a Complex MATLAB Program with Respect to Maintainability", in *Proceedings of the Huntsville Simulation Conference (HSC'08)*, J. Gauthier, Ed. San Diego, CA, USA: The Society for Modeling and Simulation, 2008, pp. 309–315.

- B. Güde, B. Krüger, M. Najafi, and D. P. F. Möller, "Spin valves in reconfigurable logic gates (poster)", in *Program and Abstracts of the International Conference on Magnetism (ICM 2009)* Karlsruhe, Germany, J. Wosnitza, L. Schultz, and J. Blügel Eds. Kalsruhe, Germany: ICM 2009 Secretary, 2009, p. 322.

Appendix E

Research stays

- M. Bolte, T. Kamionka, and B. Güde, Advanced Light Source (ALS), 9–14 April 2008, Berkeley, California, USA. Time-resolved measurements of the dynamics of vortices and antivortices due to an applied magnetic field and an electric current at beamline 11.0.2 (Scanning Transmission X-Ray Microscope).
- B. Güde, University of Glasgow, 4 August 2009–30 September 2009, Glasgow, United Kingdom. Research in the Device Modeling Group of Professor Dr. Asen Asenov. Fundamentals of modeling and simulation of semiconductor devices and the development of compact models.

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